Microarchitectural Side-Channel Attacks

Part 2

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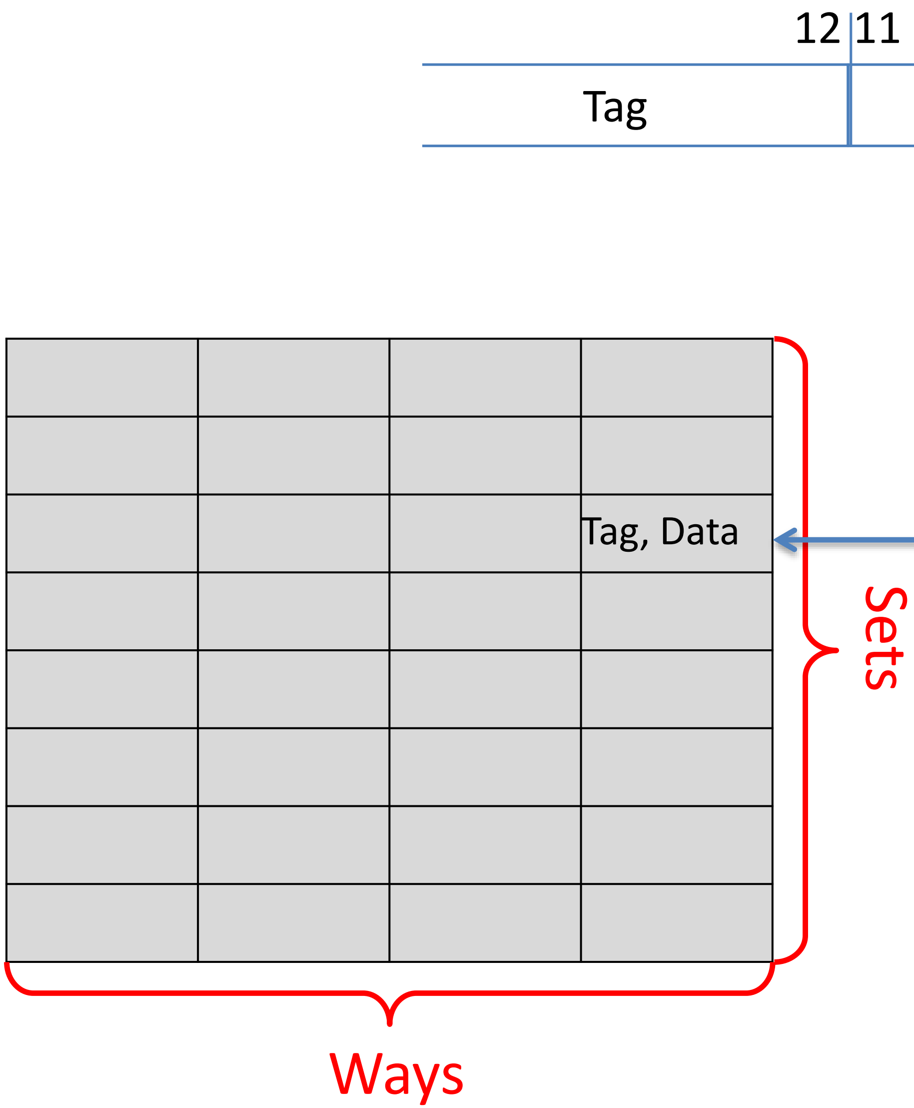
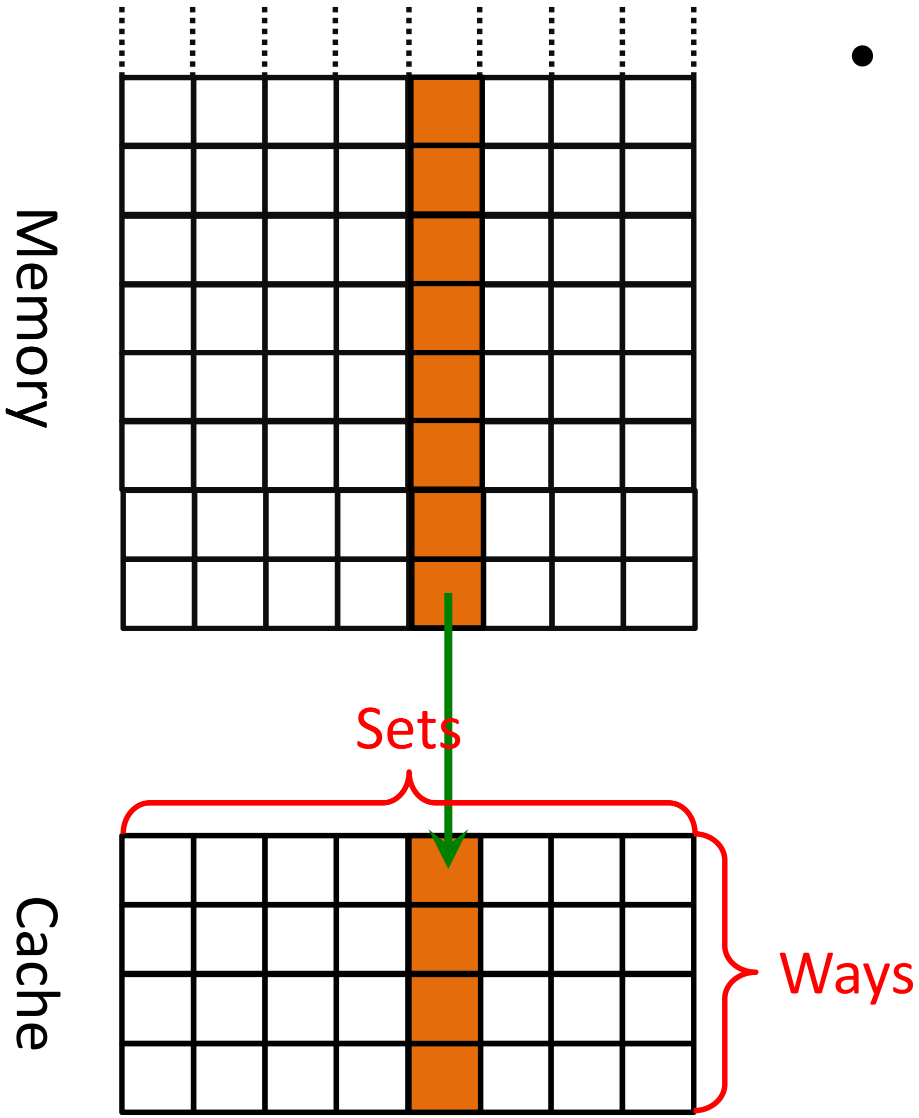
X86 L1 Cache



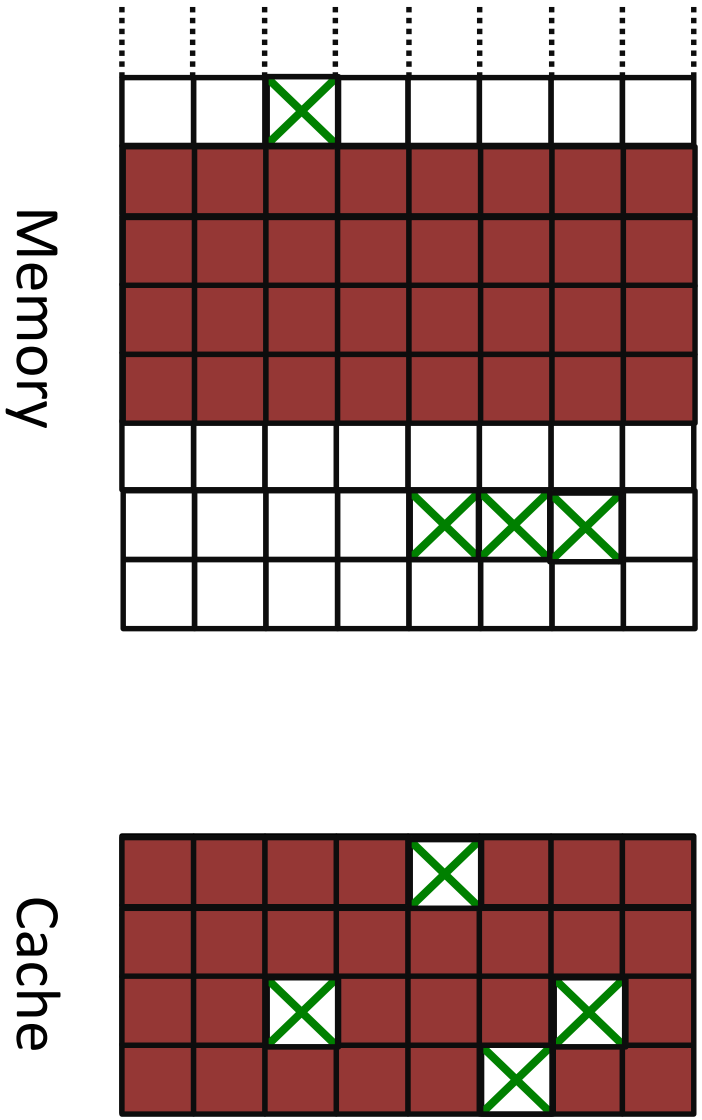
- Stores fixed-size (64B) *lines*
- Arranged as multiple (64) *sets*, each consisting of multiple (8) *ways*.
- Each memory line maps to a single cache set
  - Bits 6-11 select the set
  - Can be cached in any of the ways in the set

X86 L1 Cache



- Better visualised when the cache is rotated

Prime+Probe [OST05, Per05]



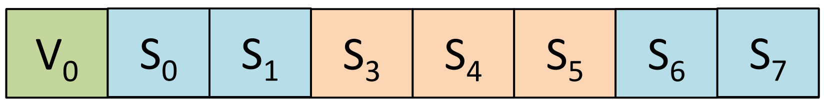
- Attacker chooses a cache-sized memory buffer
- Attacker accesses all the lines in the buffer, filling the cache with its data
- Victim executes, evicting some of the attackers lines from the cache
- Attacker measures the time to access the buffer
  - Accesses to cached lines is faster than to evicted lines

The gritty details

- The observer effect
  - Our code uses the cache - want to minimise our footprint
- The optimising compiler removes what it thinks is dead code
  - Not optimising increases the code's footprint
  - Solution:
    - Know your optimiser
    - Use assembly language

Thrashing

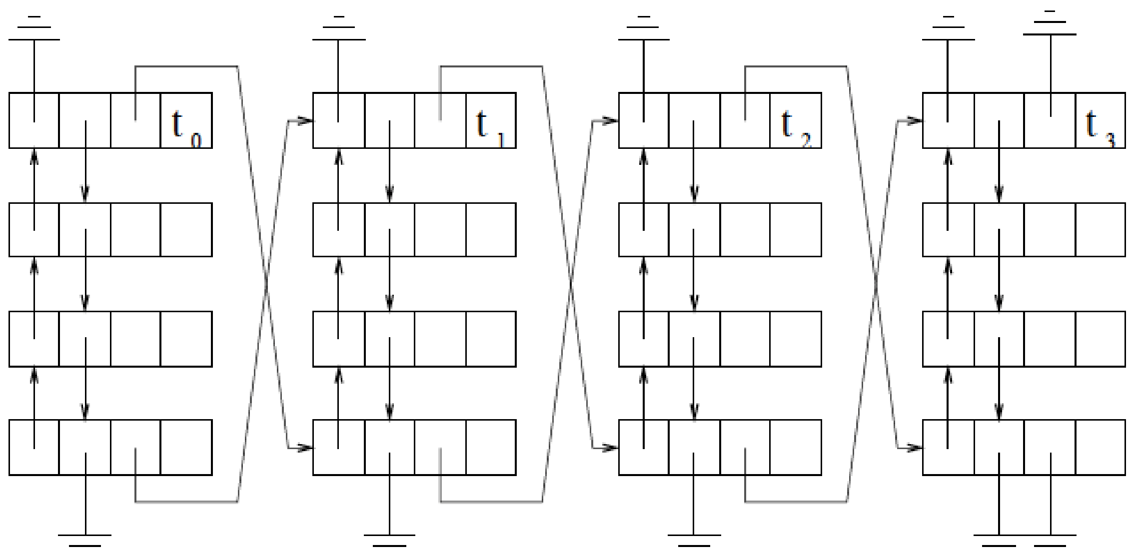
- The cache uses a Pseudo-LRU replacement
- Our probe + victim access can cause thrashing



- Solution [TOS10]: Zig-zag on data

Hardware prefetcher

- Aims to improve temporal locality
- Brings data to the cache before it is required
  - We do not want that!!!
- Solution [TOS10]: pointer chasing
  - [Per05] uses data dependency for achieving the same result



Data streams

- The cache aims to predict regular access patterns with fixed strides
- Linear access within a page may trigger the mechanism
- Solution [OST10]: Randomise order of probed sets

Putting it all together

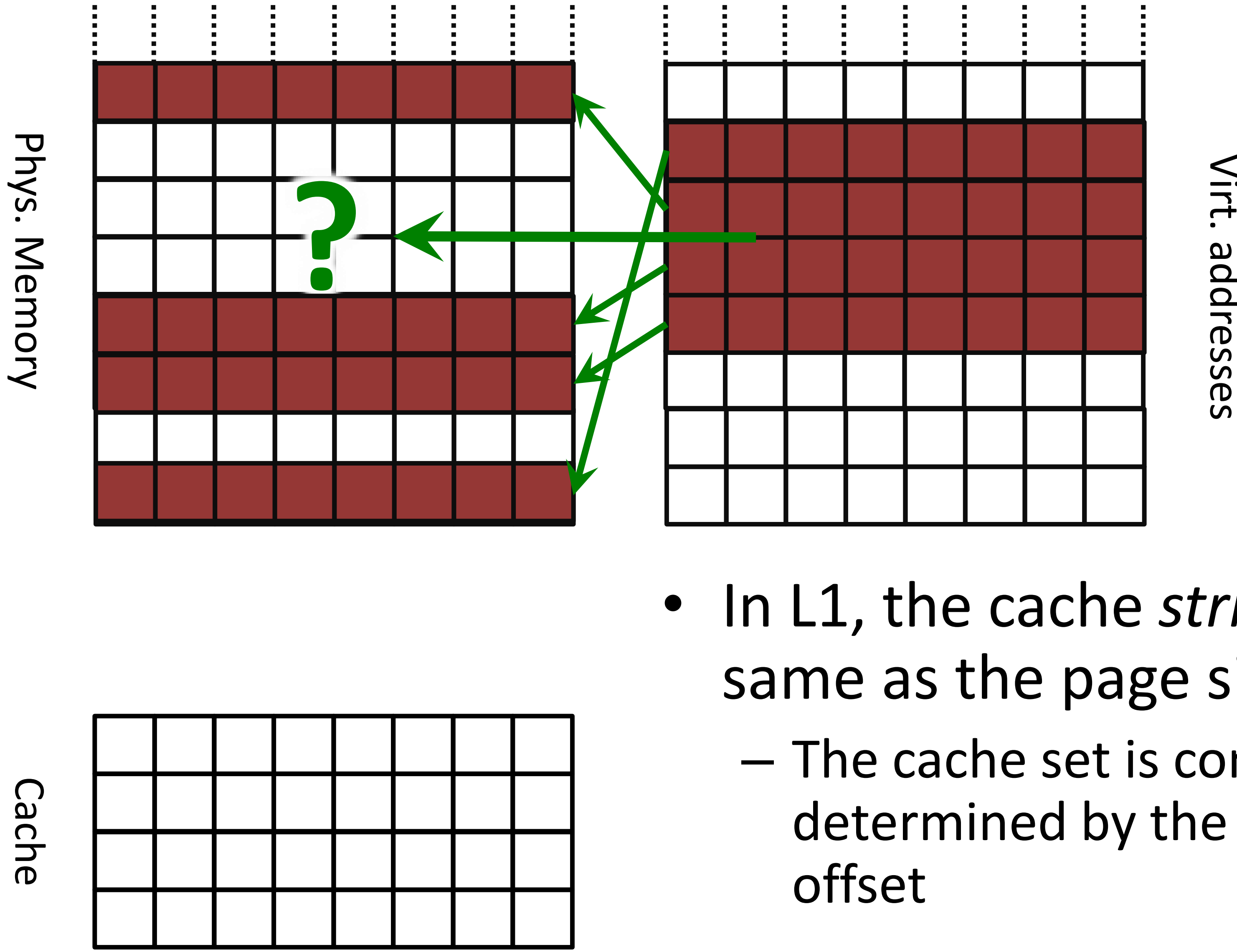
- L1-capture

- With L1-rattle
- With rungnupg

Challenges to last-level cache attacks

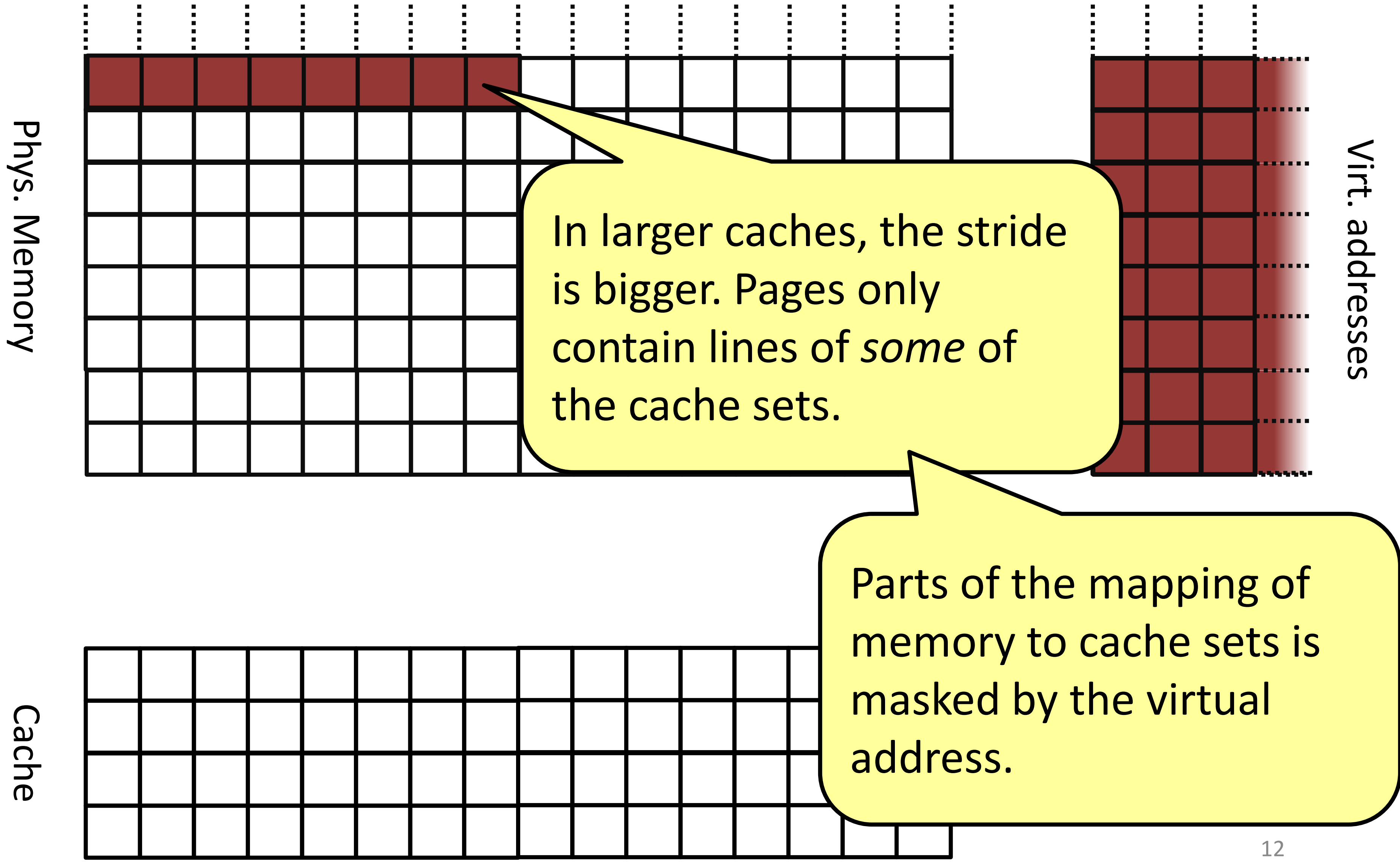
- Difficulty in finding memory lines that map to a given cache set
  - Virtual memory
  - LLC slices
- Large cache size and longer cache access times mean LLC Prime+Probe is very slow
- Visibility of the victim memory access at the LLC
  - Intel inclusive cache takes care of the issue

Virtual vs. Physical addresses

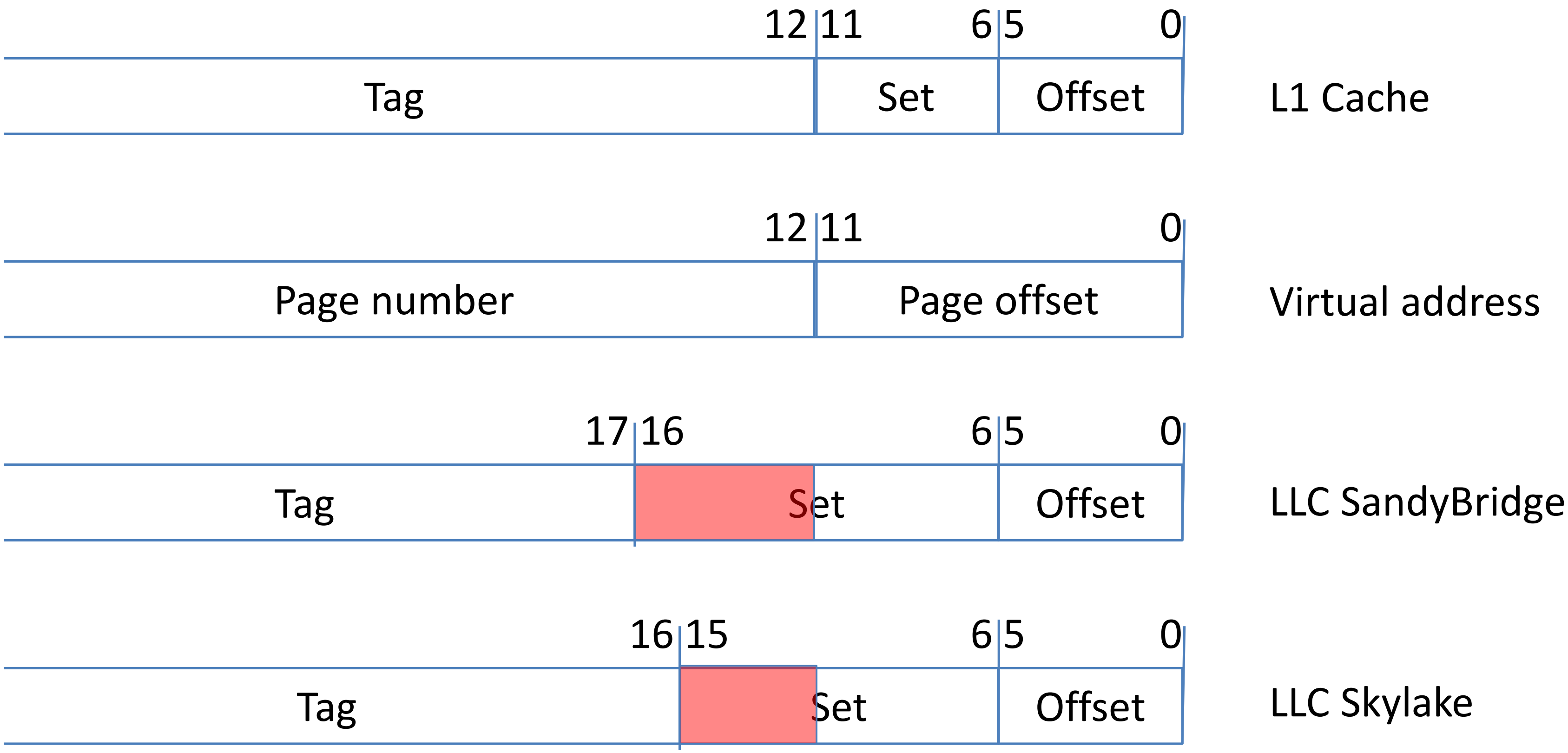


- In L1, the cache *stride* is the same as the page size (4KiB)
  - The cache set is completely determined by the page offset

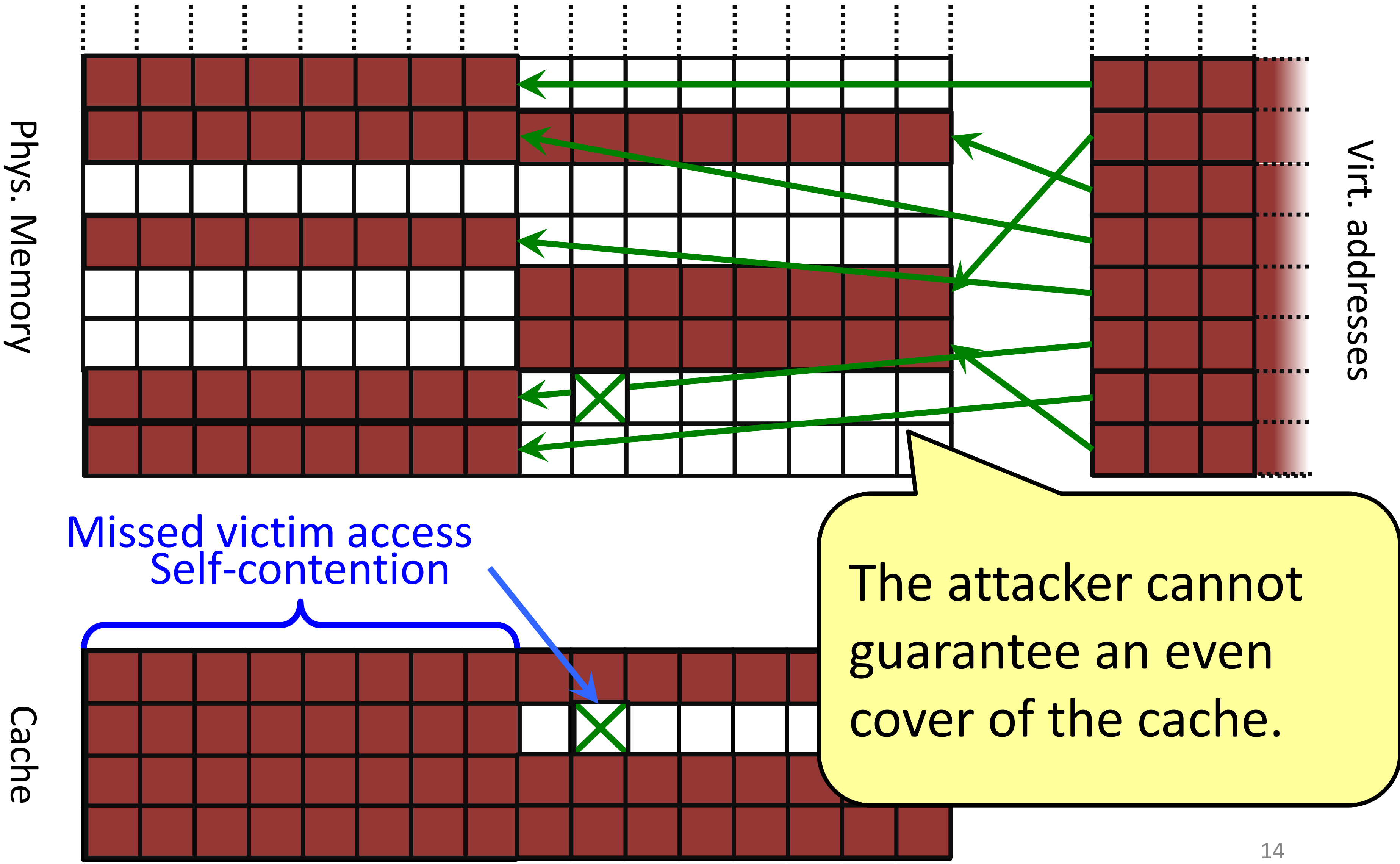
Addressing uncertainty



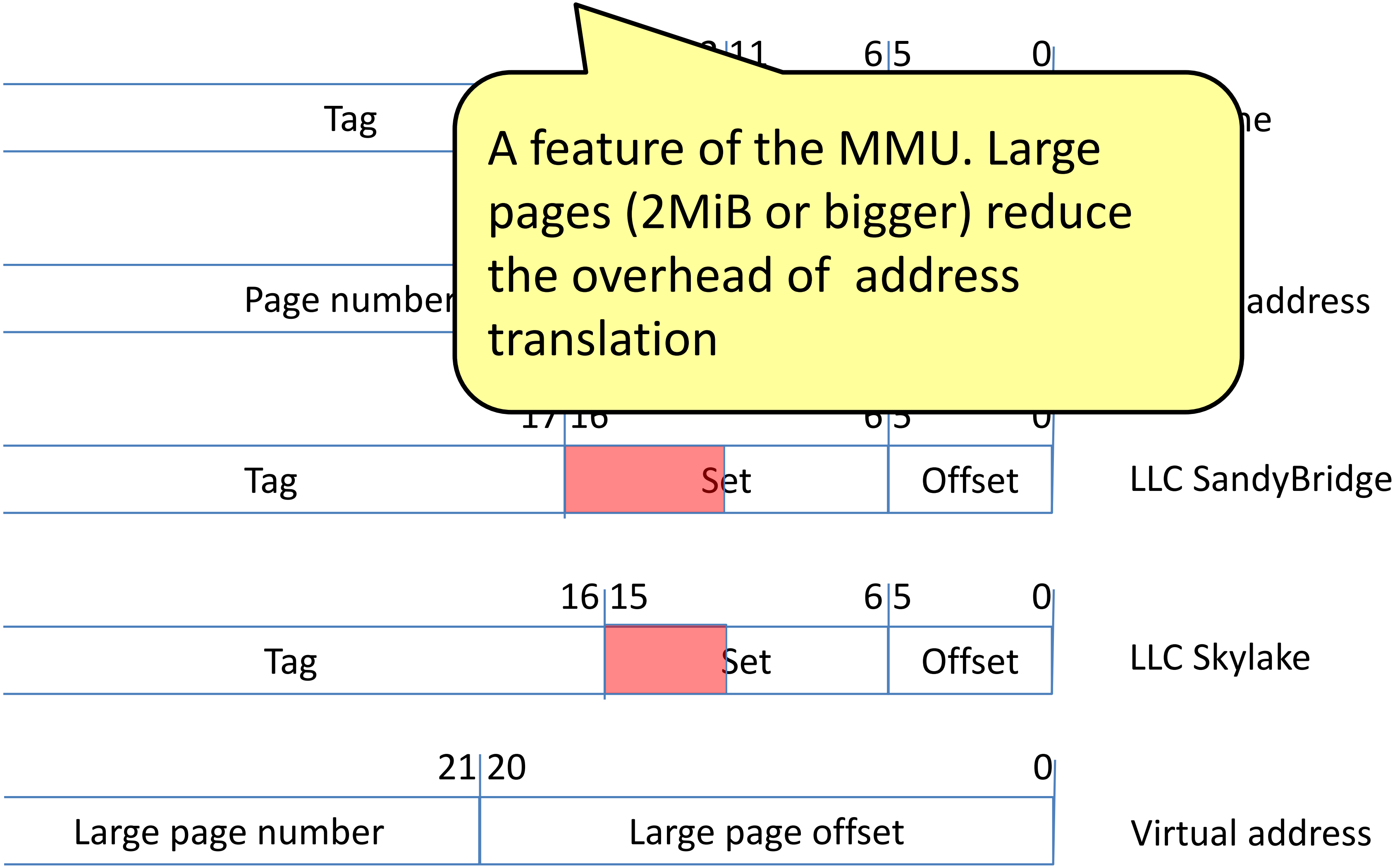
Address fields



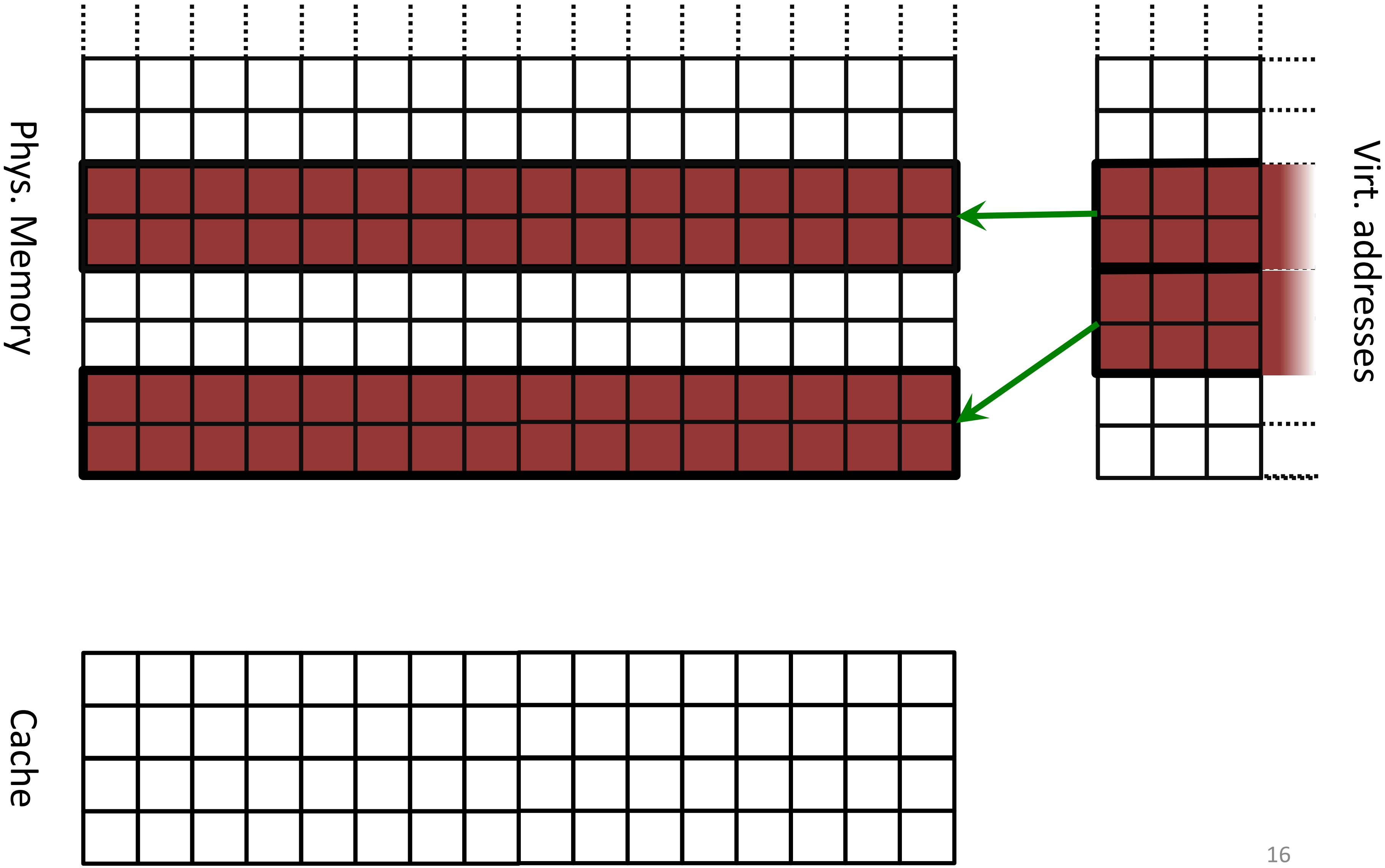
Addressing uncertainty



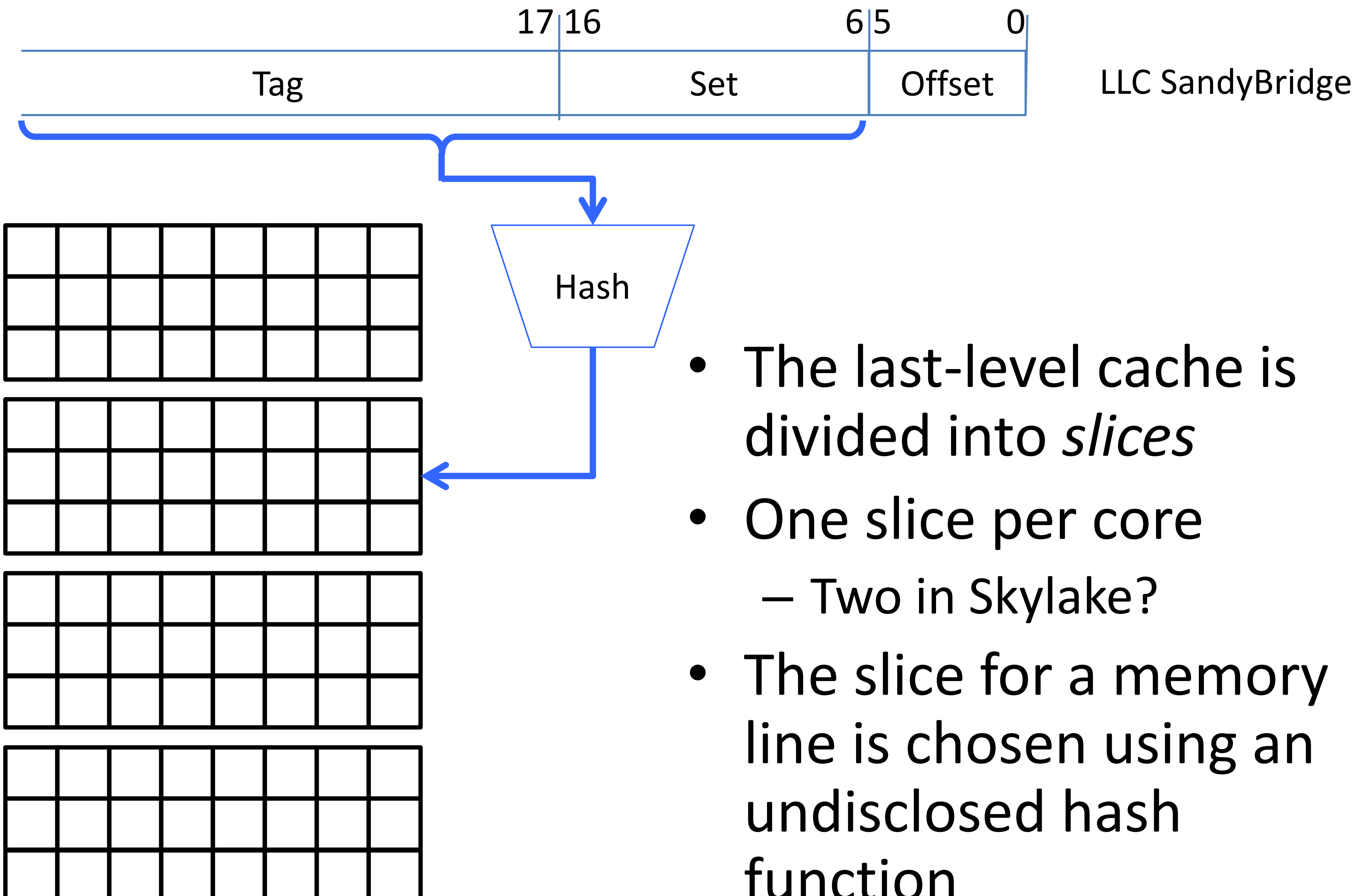
Solution : Use large pages [LYG+15,IES15]



Solution – large pages



Intel LLC Slices



- The last-level cache is divided into *slices*
- One slice per core
  - Two in Skylake?
- The slice for a memory line is chosen using an undisclosed hash function

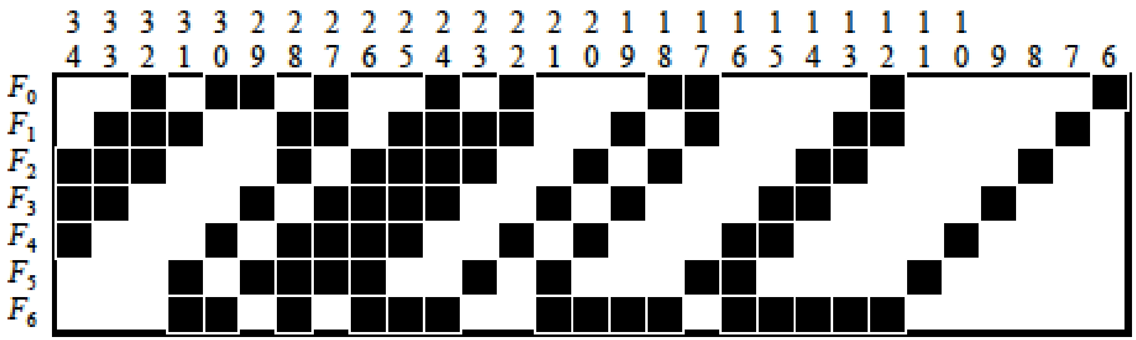
Reverse Engineering the Hash Function

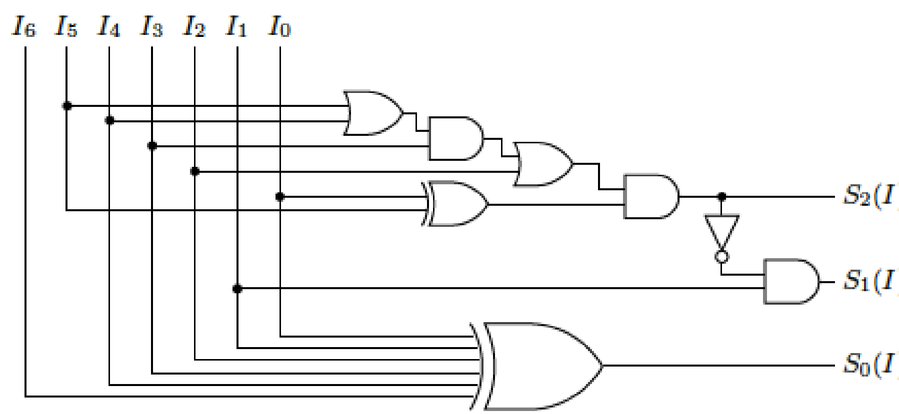
- [MLN+15] Use performance counters to RE linear hash functions (number of cores is a power of two)

		Address Bit																															
		37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06
2 cores	o_0						⊕		⊕		⊕	⊕	⊕	⊕	⊕		⊕		⊕		⊕	⊕	⊕		⊕		⊕		⊕				⊕
4 cores	o_0					⊕	⊕		⊕		⊕	⊕	⊕	⊕	⊕		⊕		⊕		⊕	⊕	⊕		⊕		⊕		⊕				⊕
	o_1				⊕	⊕		⊕		⊕	⊕		⊕		⊕	⊕	⊕	⊕	⊕	⊕		⊕		⊕		⊕		⊕				⊕	
8 cores	o_0		⊕	⊕		⊕	⊕		⊕		⊕	⊕	⊕	⊕	⊕		⊕		⊕		⊕	⊕	⊕		⊕		⊕		⊕				⊕
	o_1	⊕		⊕	⊕	⊕		⊕		⊕	⊕		⊕		⊕	⊕	⊕	⊕	⊕	⊕		⊕		⊕		⊕		⊕				⊕	
	o_2	⊕	⊕	⊕	⊕			⊕	⊕			⊕	⊕			⊕	⊕			⊕			⊕			⊕	⊕				⊕		

Reverse Engineering the Hash Function

- [YGL+15] use timing to RE the function for 6 cores





Reverse Engineering the Hash Function

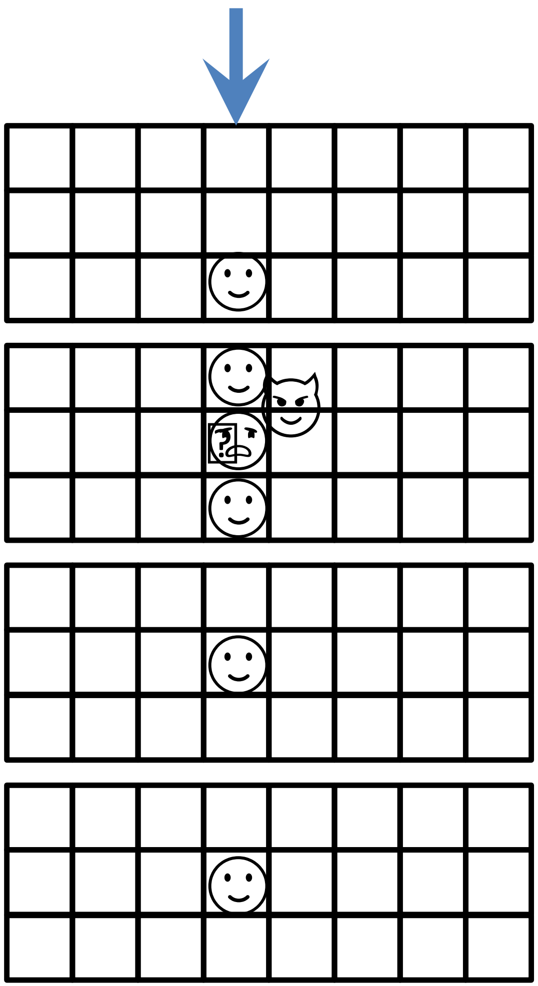
- [MLN+15] Use performance counters to RE linear hash functions (number of cores is a power of two)
- [YGL+15] use timing to RE the function for 6 cores

- But – need physical addresses
  - Can be done on Linux < 4.0
  - Unless running in a VM

Probing the hash function

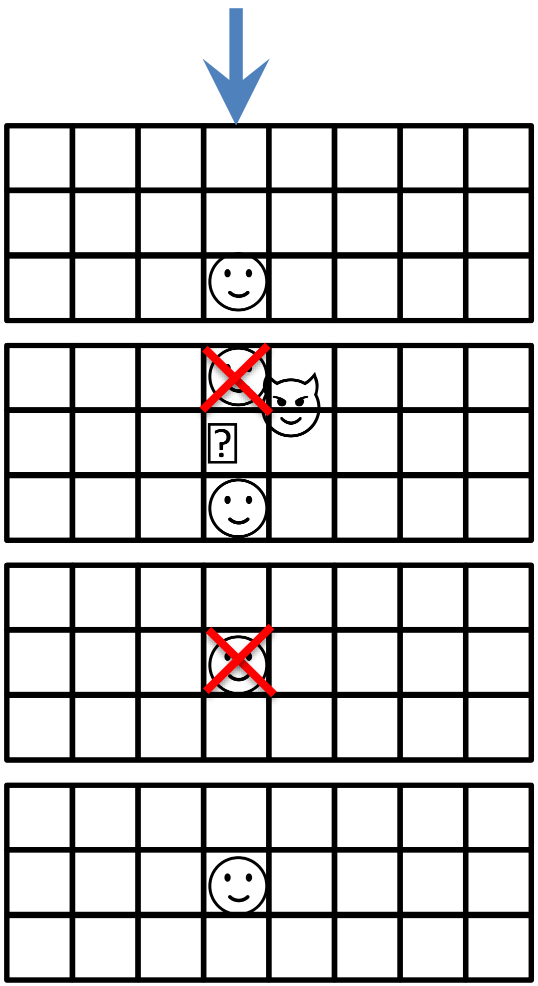
- Start with a set of potentially conflicting memory lines
  - At least twice as many as the totalsize of the cache sets
- *Expand* a subset until it conflicts on a single set in a single slice
- *Contract* the subset until it contains only lines of the conflicted set
- *Collect* all of the lines of the conflicting set from the original set
- Repeat until the original set is (almost) empty

Expand



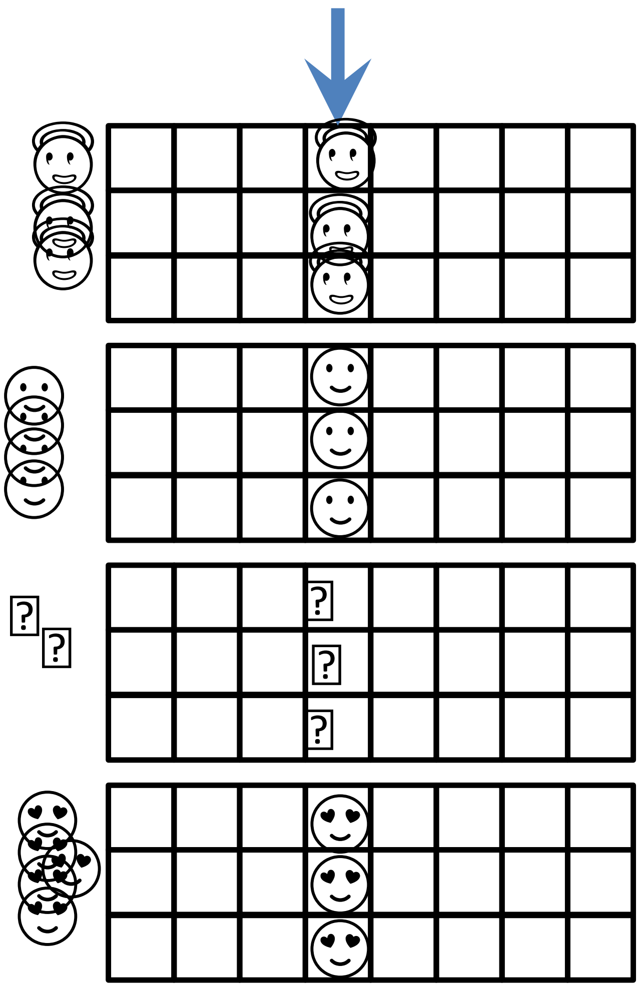
- Start from an empty subset
- Iteratively add lines to the subset as long as there is no self-eviction
- Self-eviction is detected by priming a potential new member, accessing the current subset and timing another access to the potential new member

Contract



– Iteratively remove lines from the subset checking for self-eviction
– Only keep members if self-eviction disappears when removed

Collect



– Scan original set, looking for members that conflict with the contracted subset

Demo

- L3-capture
- L3-capturecount

Slow LLC Prime+Probe times

- L1 (32KB) probe:
  - 64 sets * 8 ways *4 cycles = 2,048 cycles
- Small last-level cache (6MB):
  - 8,192 sets * 12 ways * ~30 cycles = ~3,000,000 cycles
- We cannot probe the entire LLC in a reasonable time, but probing one cache set is fast
- Our solution:
  - Probe one or a few cache sets at a time
  - Look for temporal patterns rather than spatial footprints

Demo

- L3-scan

Countermeasures

- Hardware
- System
- Software

Hardware countermeasure

- Don't share
- Hardware cache partitioning [DJL+12]
  - Intel Cache Allocation Technology
- Cache Randomisation [WL06]

System Countermeasures

- Limited sharing
  - Don't share memory
  - Don’t share cores
- Cache Colouring [BLRB94,SSCZ11]
  - STEALTHMEM [KPM12]
- CATalyst [LGY+16]
- CacheBar [ZRZ16]

Software Countermeasures

- Constant-time programming
  - No variable-time instructions
  - No secret-dependent flow control
  - No secret-dependent memory access

Non constant-time [YB14]

```
for (; i >= 0; i--)
    {
    word = scalar->d[i];
    while (mask)
        {
        if (word & mask)
            {
            if (!gf2m_Madd(group, &point->X, x1, z1, x2, z2, ctx)) goto err;
            if (!gf2m_Mdouble(group, x2, z2, ctx)) goto err;
            }
        else
            {
            if (!gf2m_Madd(group, &point->X, x2, z2, x1, z1, ctx)) goto err;
            if (!gf2m_Mdouble(group, x1, z1, ctx)) goto err;
            }
        mask >>= 1;
        }
    mask = BN_TBIT;
    }
```

Constant-time

```
for (; i >= 0; i--) {
    word = scalar->d[i];
    while (mask) {
        BN_consttime_swap(word & mask, x1, x2, group->field.top);
        BN_consttime_swap(word & mask, z1, z2, group->field.top);
        if (!gf2m_Madd(group, &point->X, x2, z2, x1, z1, ctx))
            goto err;
        if (!gf2m_Mdouble(group, x1, z1, ctx))
            goto err;
        BN_consttime_swap(word & mask, x1, x2, group->field.top);
        BN_consttime_swap(word & mask, z1, z2, group->field.top);
        mask >>= 1;
    }
    mask = BN_TBIT;
}
```

Constant-time

```
    assert((condition & (condition - 1)) == 0);
    assert(sizeof(BN_ULONG) >= sizeof(int));

    condition = ((condition - 1) >> (BN_BITS2 - 1)) - 1;

    t = (a->top ^ b->top) & condition;
    a->top ^= t;
    b->top ^= t;

#define BN_CONSTTIME_SWAP(ind) \
        do { \
                t = (a->d[ind] ^ b->d[ind]) & condition; \
                a->d[ind] ^= t; \
                b->d[ind] ^= t; \
        } while (0)

    switch (nwords) {
    default:
        for (i = 10; i < nwords; i++)
            BN_CONSTTIME_SWAP(i);
        /* Fallthrough */
    case 10:
        BN_CONSTTIME_SWAP(9);   /* Fallthrough */
    case 9:
        BN_CONSTTIME_SWAP(8);   /* Fallthrough */
```

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