Efficient Power and Timing Side Channels for Physical Unclonable Functions

CHES, September 26, 2014

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M. Majzoobi (d), F. Koushanfar (d), W. Burleson (b)

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(c) Freie Universität Berlin, (d) Rice University
(*) These authors contributed equally

Outline

1. **Background: The Arbiter PUF Family, Pure Modeling Attacks, and Their Limitations**
2. Power and Timing Side Channels on XOR Arbiter PUFs
3. Combining Side Channels with Modeling Attacks
4. Our Results
5. Summary

Physical Unclonable Functions (PUFs)

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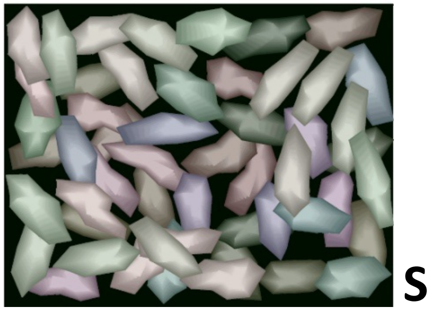
External Stimuli/ **Challenges C_i**

PUF
(= (partly) disordered, unclonable physical system S)



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(R_i is a function of the applied challenge C_i and the specific disorder in S)

(C_i , R_i): Challenge-response pairs **(CRPs)** of the PUF

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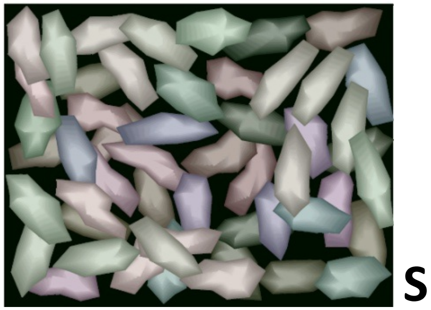

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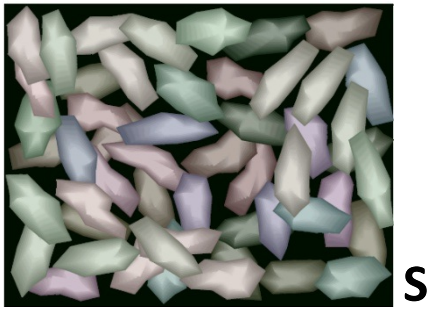

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- Challenge-response interface is publicly accessible
  - **Everyone** who holds physical possession of the Strong PUF can freely apply challenges and read out responses

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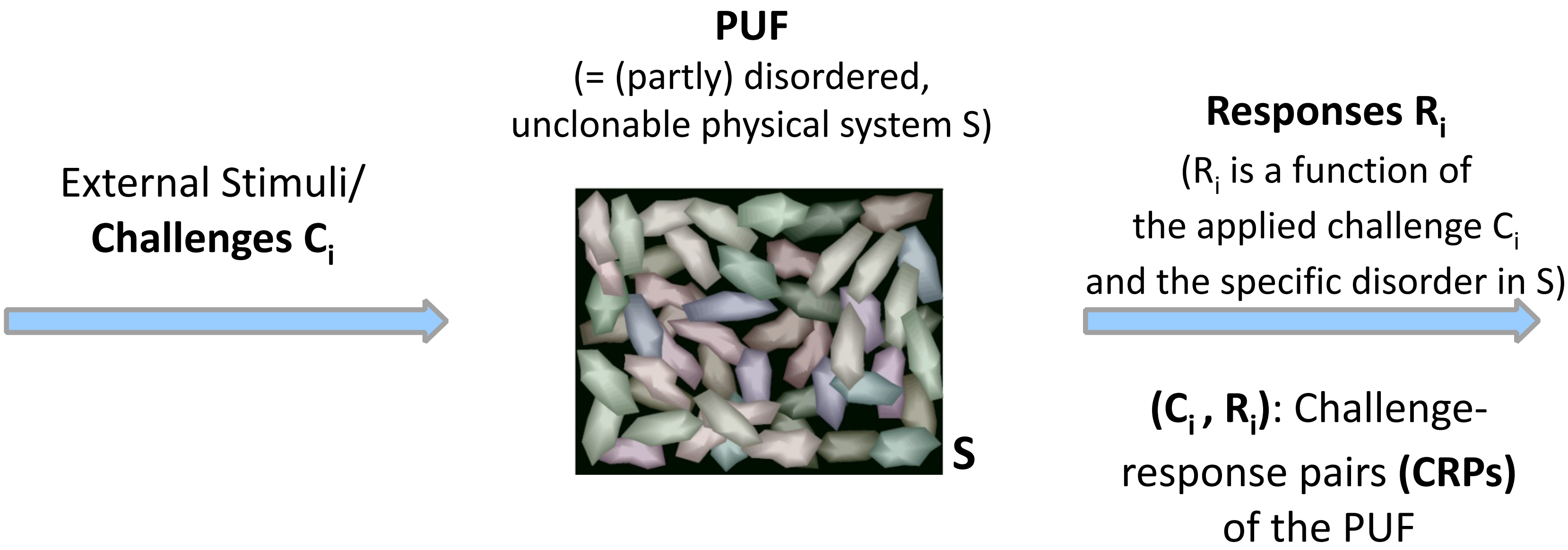

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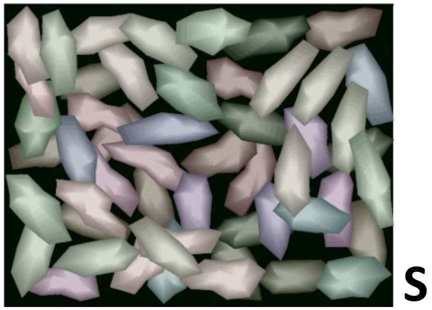

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- Very many possible challenges *(ideally exponentially many)*
- Complex: No numerical prediction of unknown responses

The most widespread electrical Strong PUF: **Arbiter PUFs** (1)

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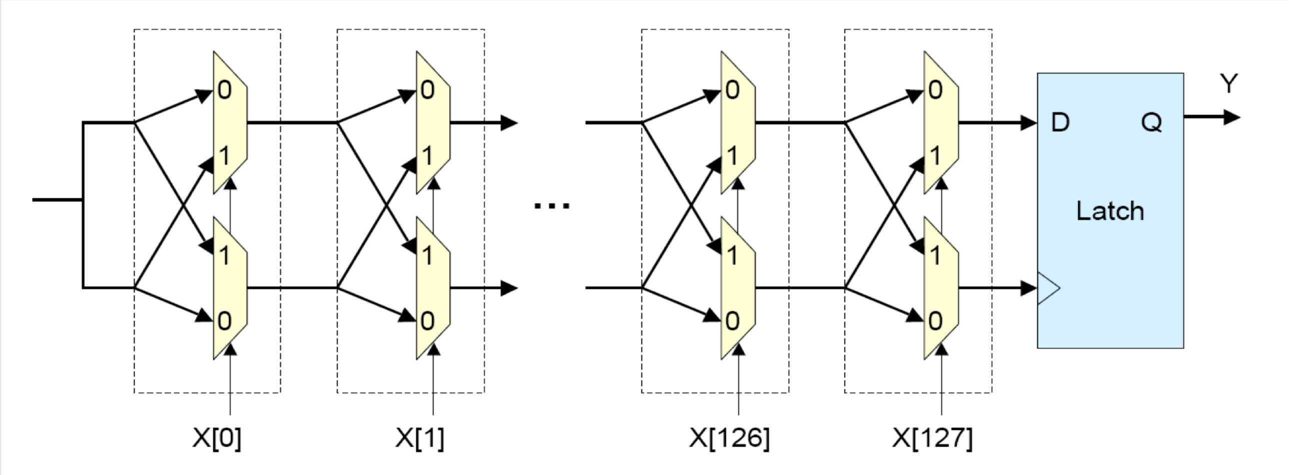

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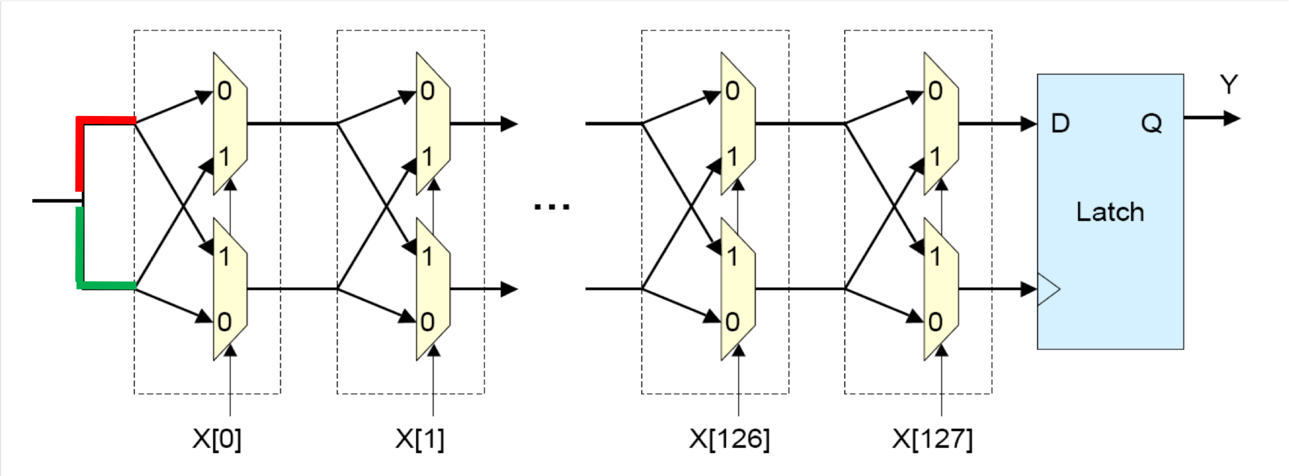

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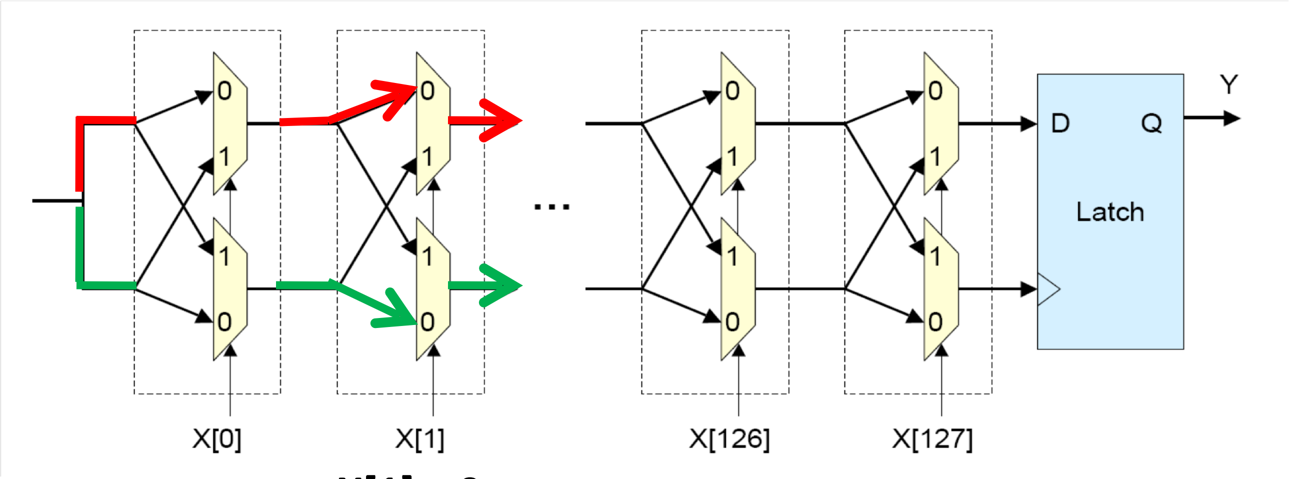

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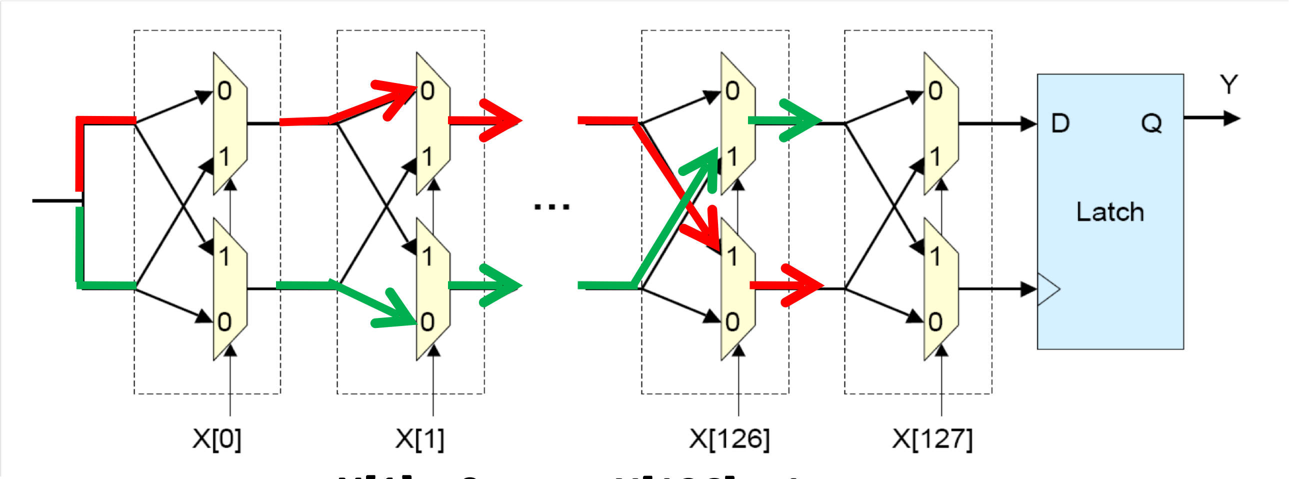

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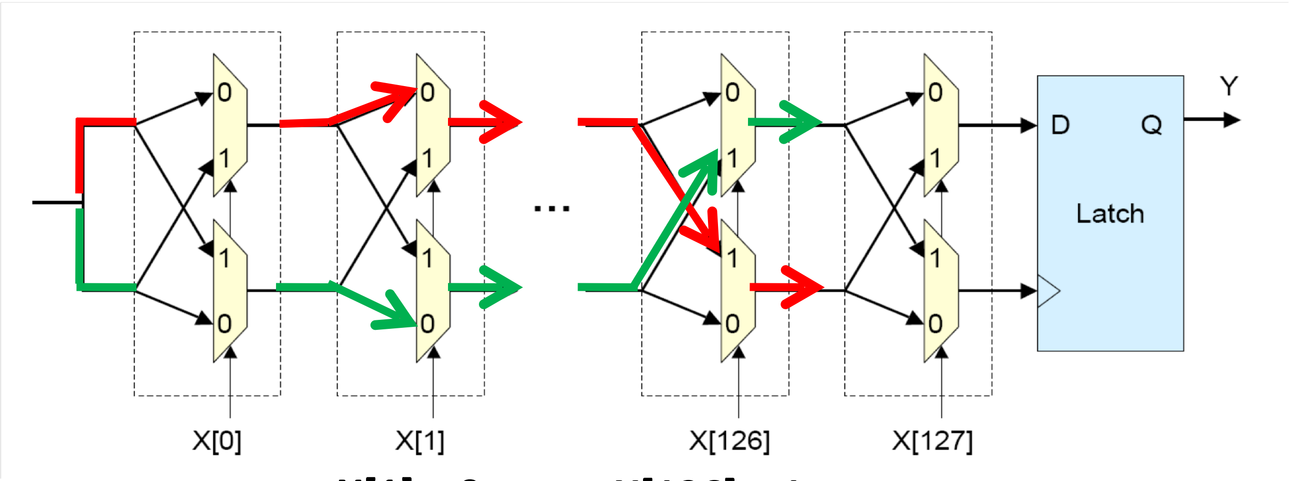

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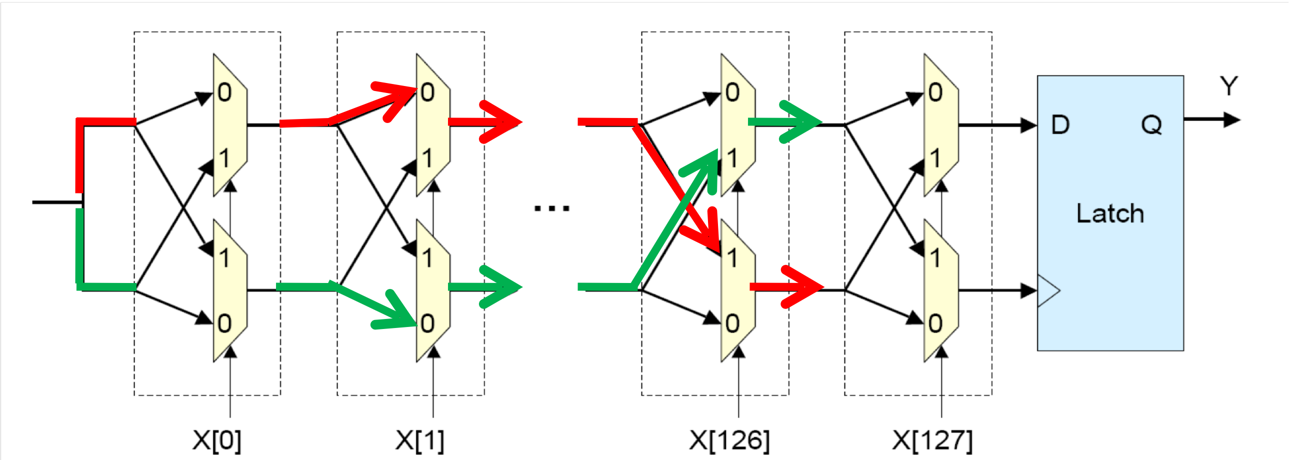

X[1] = 0　　**X[126] = 1**

- ***But: Linear!***
- Adversaries can derive the internal delays via machine learning techniques (in so-called ***„modeling attacks“***) (2)
  – **Complexity of attacks:** *Linear* no. of CRPs, *quadratic* runtime

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Enhanced Designs of the Arbiter PUF Family

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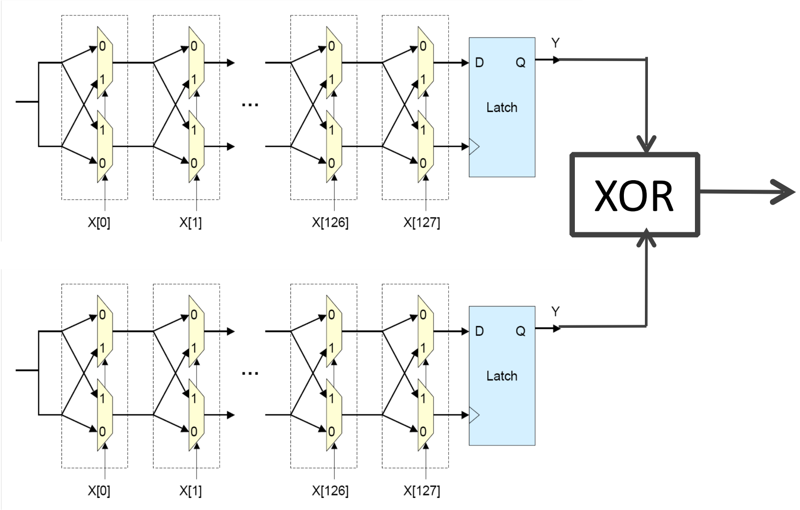
k-XOR Arbiter PUF

G. Suh et al, DAC 2007



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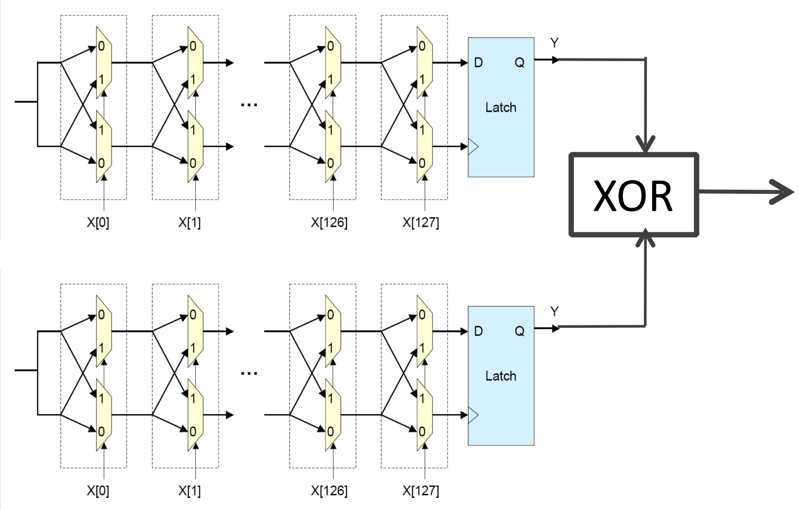

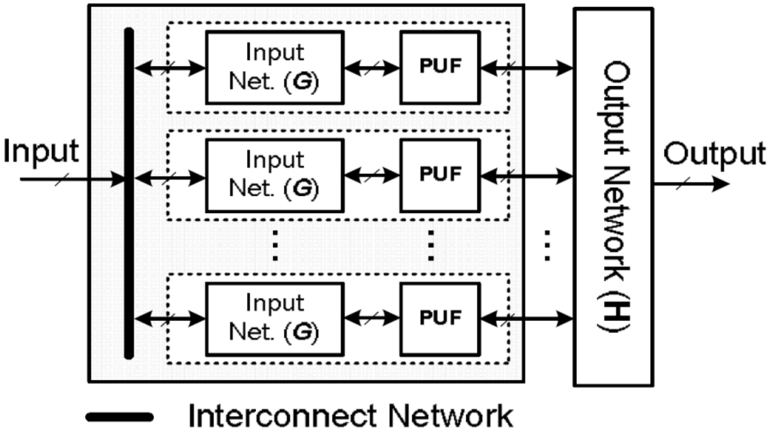

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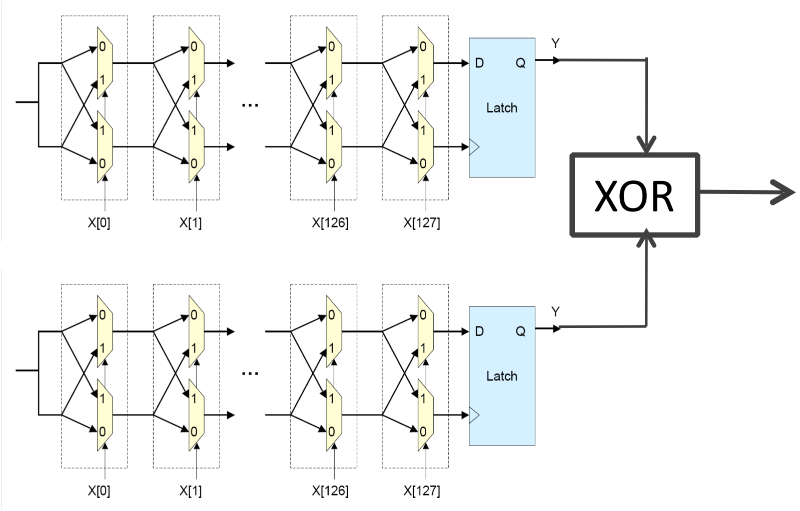

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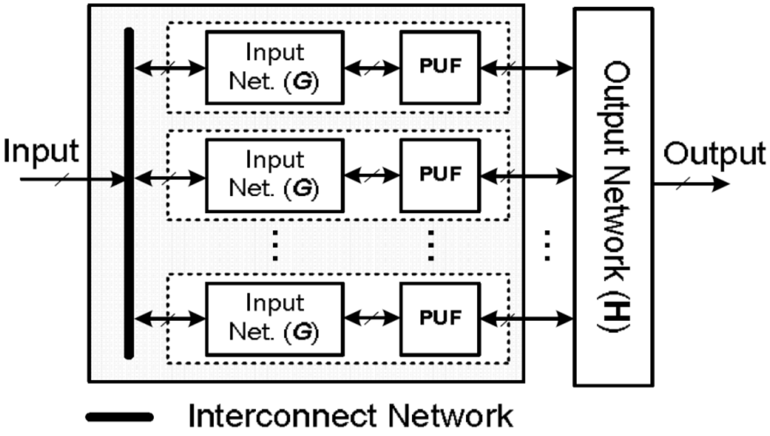

- Both XOR-based… (Also output network of LW PUF is XOR-based)

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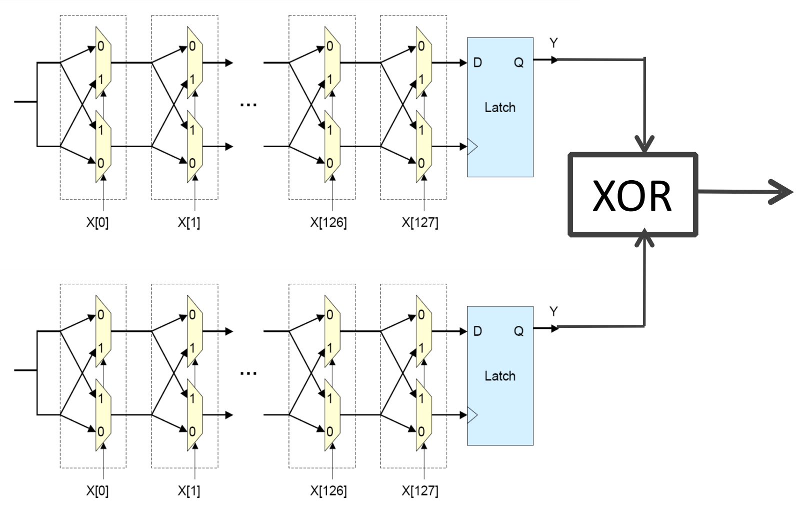

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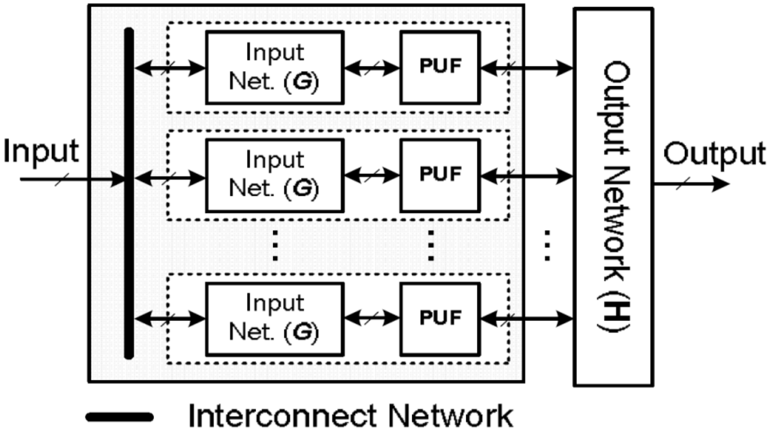

- Both XOR-based… (Also output network of LW PUF is XOR-based)
- ***„Most secure“ members of the Arbiter PUF family!*** (1,2)
  - All others have been broken (1,2)

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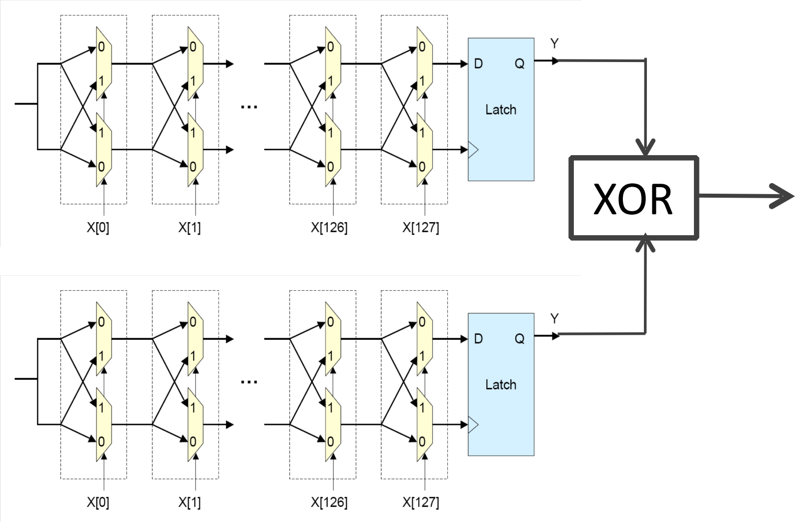

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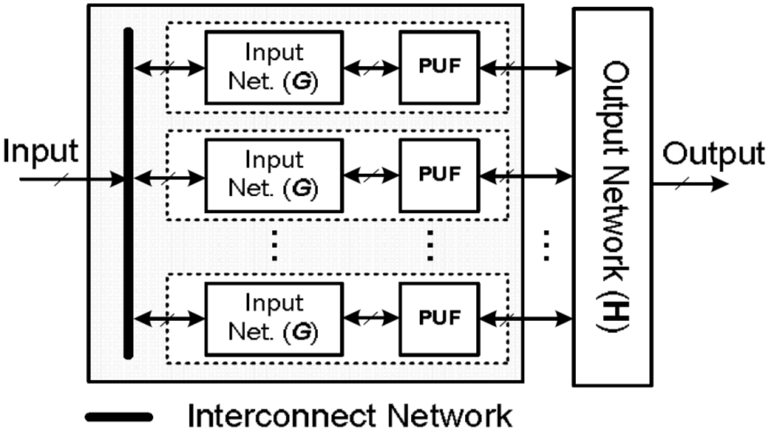

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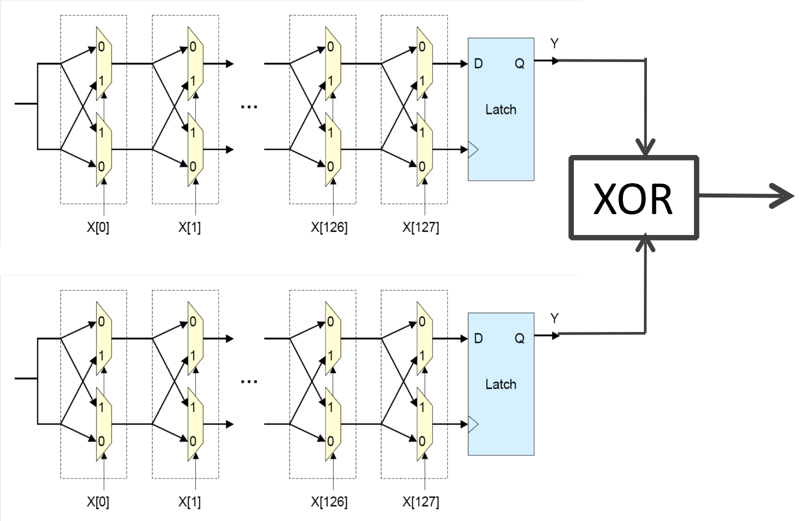

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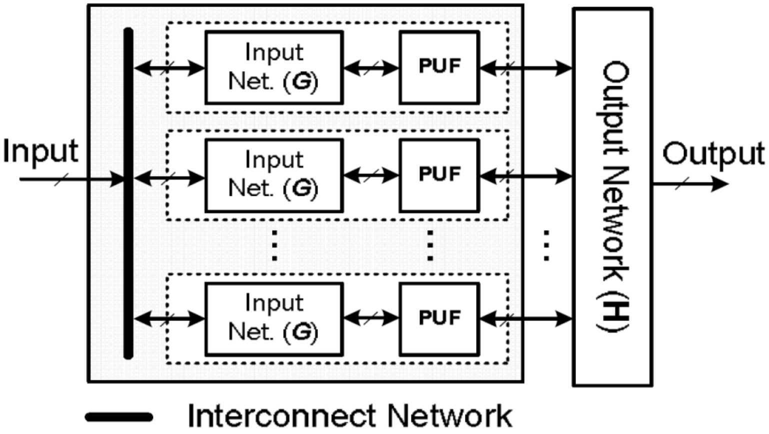

- ***How secure?***
  - Modeling attacks have **exponential** complexity (in no. of XORs) (1,2)
    - Downside: Also **exponentially bad** stability (in no. of XORs)...
  - 8 XORs **explicitly recommended as secure in literature** (1,2)

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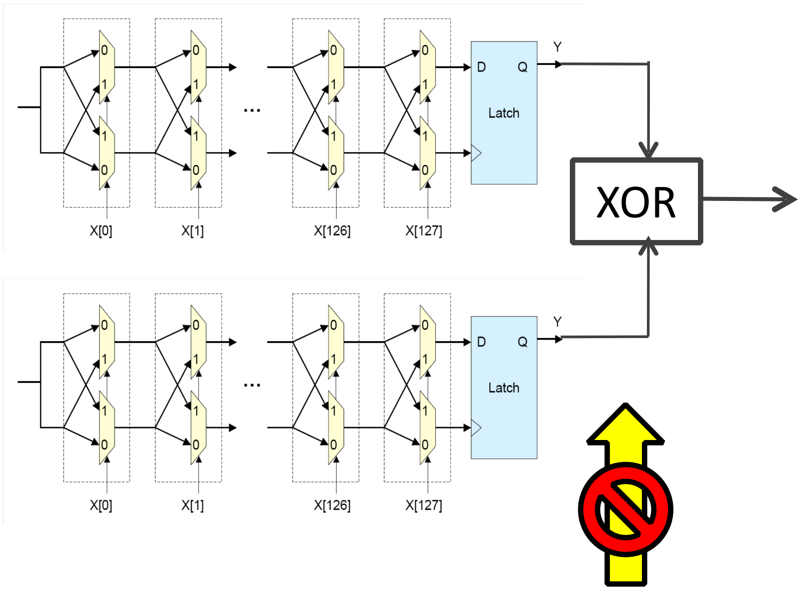

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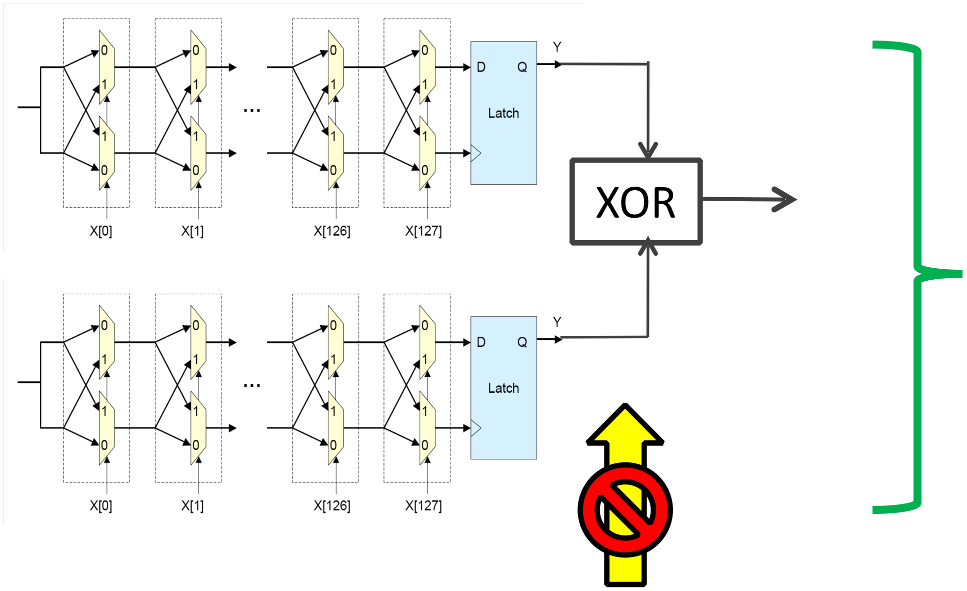

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Since direct access is difficult, we measure a global parameter instead:

The cumulative number of ones (and zeros)
in the individual outputs
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For example: In an 8 XOR Arbiter PUF, 5 individual ouputs are one, 3 are zero
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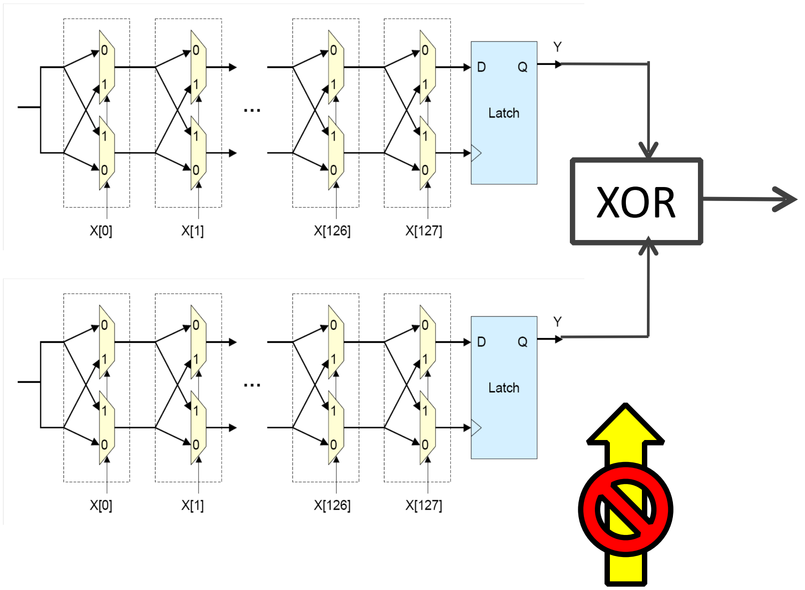

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- ***Either by power analysis or by timing analysis…***

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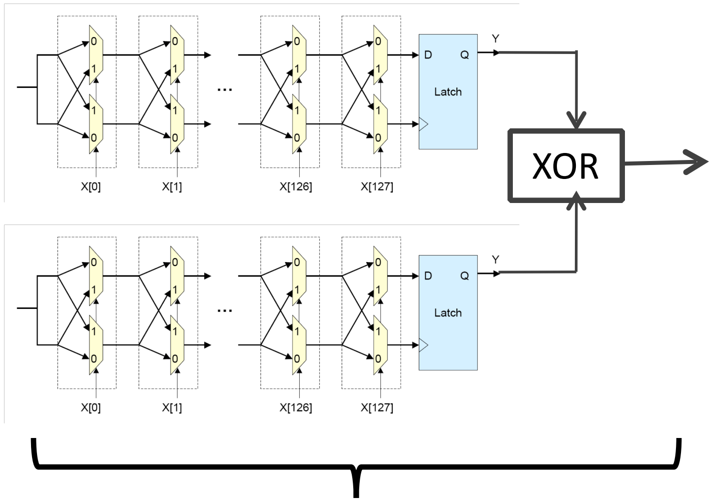
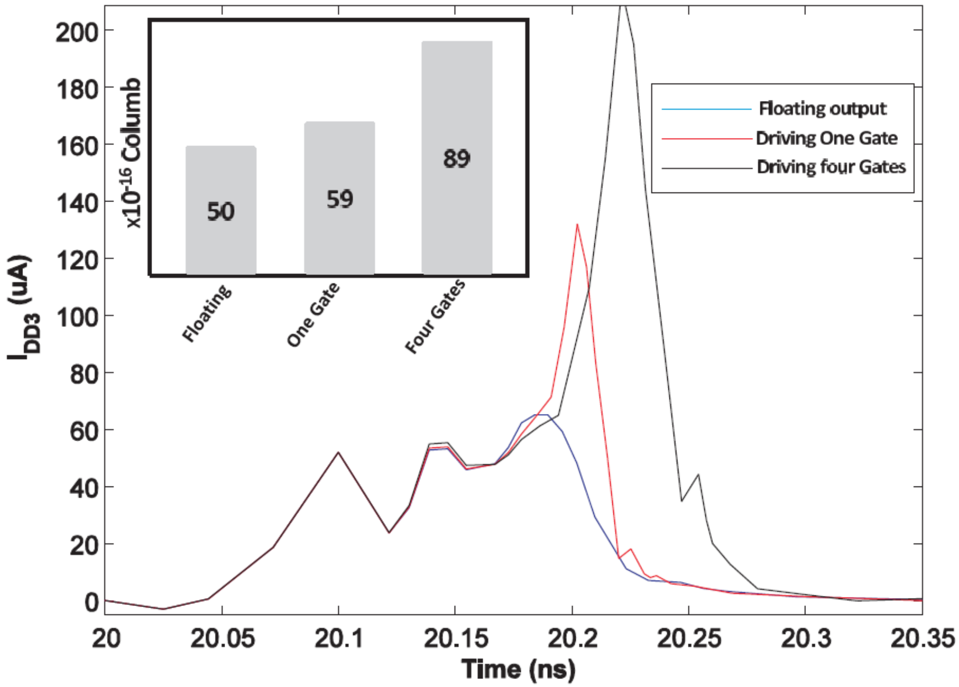


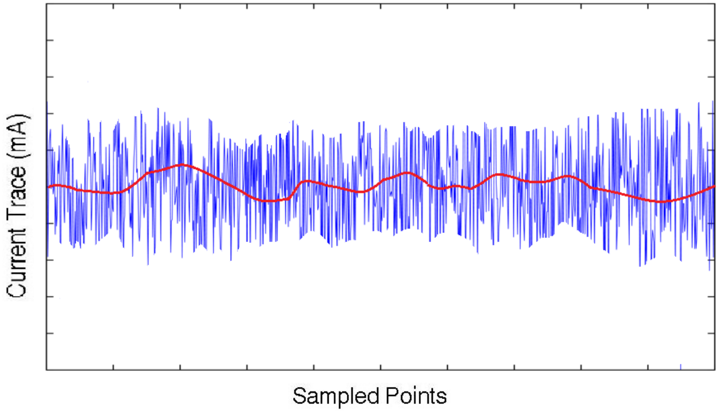
Measure „global“ power consumption



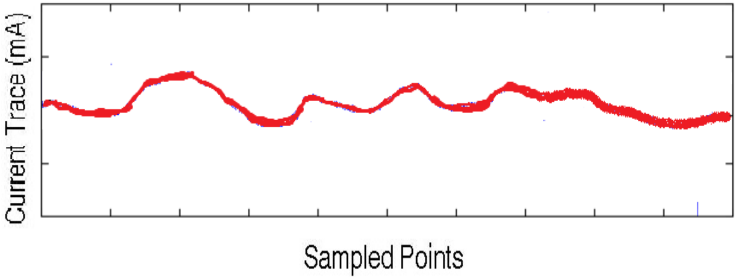
Power Side Channel (PSC) and Noise

- The PUF embedding device has other parts that draw power
- Can we isolate the effect of the latches?
  - Develop **specialized statistical technique** in the paper: Repeat measurements, analyze probability distribution

Power trace of the whole design



Power SC info we want



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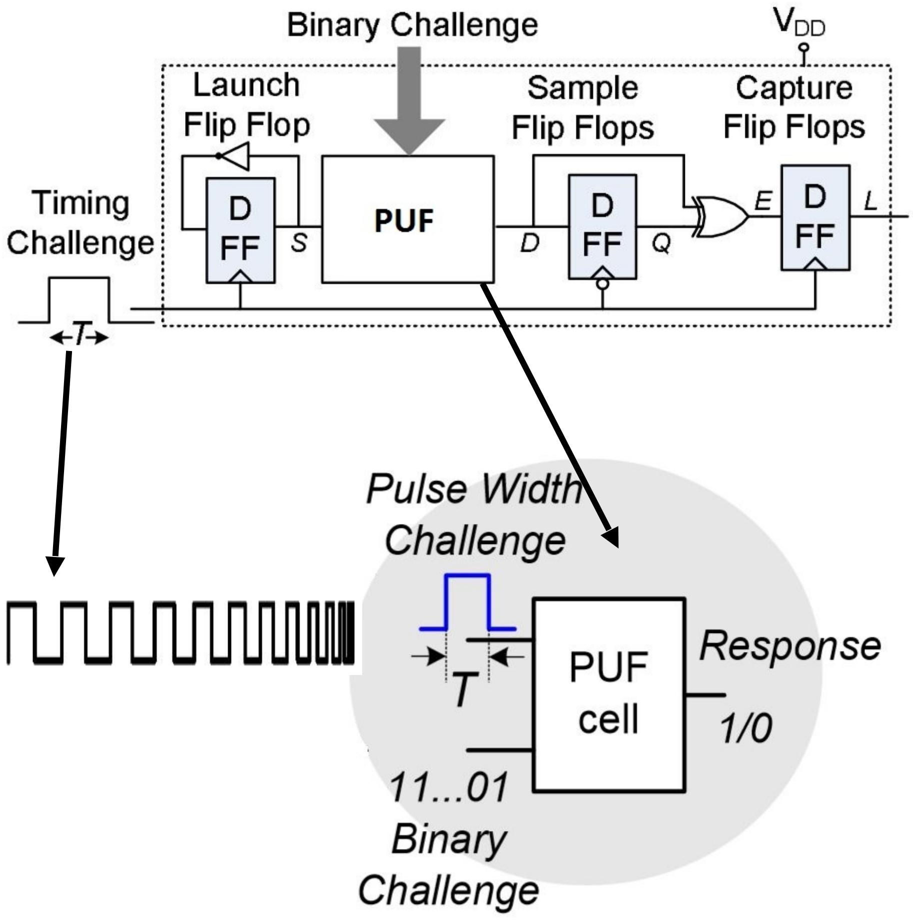

TSC extraction schematic [1]

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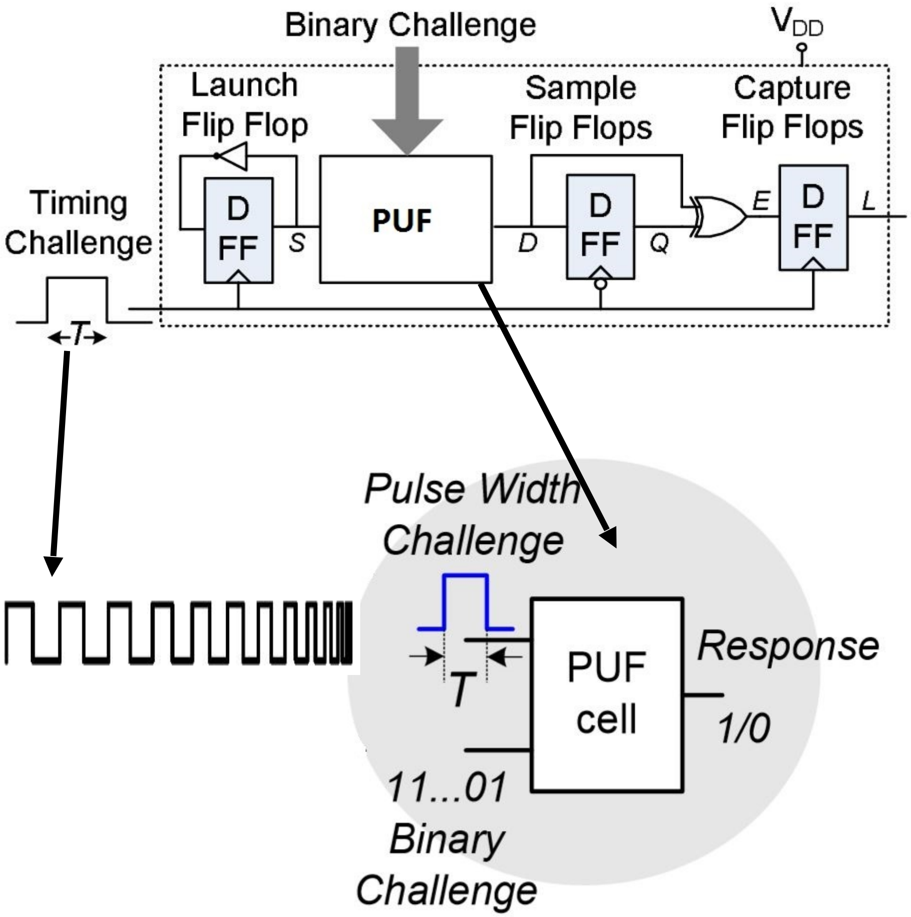

- Sweep clock to approximate the timing of XOR inputs
- Toggle will be created by changes from individual Arbiter PUFs
- Estimate the number of flipping XOR inputs with a good probability

TSC extraction schematic [1]

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- **Power SC:** Requires only an FPGA board and an oscilloscope, measurement of one CRP and side channel info takes about 1ms.

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- At first sight, the **cumulative** number of zeros/ones appears **useless**…
  - No straightforward relevance for the underlying machine learning (ML) problem…
- *It requires a **„tailormade“ ML approach** to exploit this info*
  - Quite non-trivial…
  - One of the main contributions of the paper
  - Summary over next two slides
  - Details: See paper

Machine Learning and Side Channels

(1) Rührmair et al., CCS 2010 (2) Rührmair et al., T-IFS 2013

Machine Learning and Side Channels

- General model for i-th Arbiter PUF within k-XOR Arbiter PUF (1,2):

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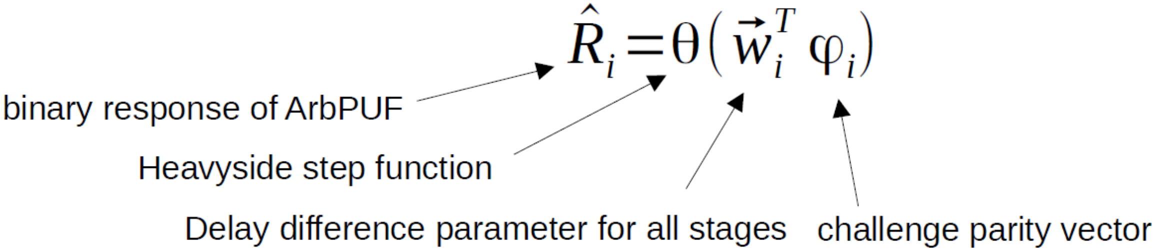

$$\hat{R}_i = \theta\left(\vec{w}_i^{\,T}\,\varphi_i\right)$$

binary response of ArbPUF

Heavyside step function

Delay difference parameter for all stages

challenge parity vector

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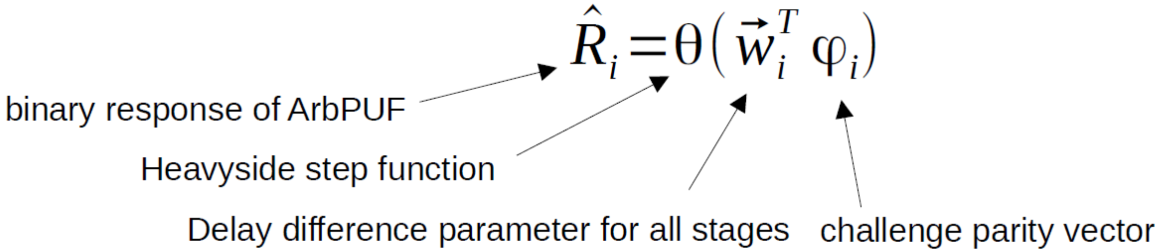

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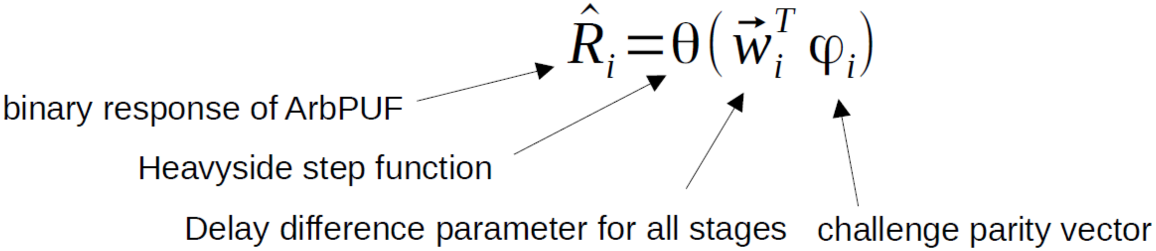

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- **Optimize** PUF-model ***w*** and minimize prediction error ***l*** :

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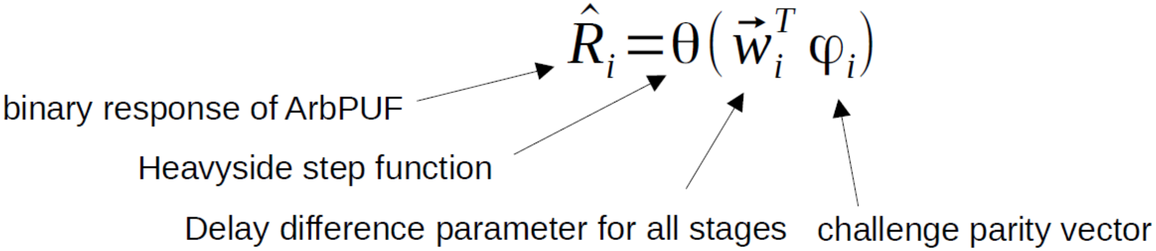

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- **Optimize** PUF-model ***w*** and minimize prediction error ***l*** :

$$l(\vec{w}, CRPs) = \sum_{(C,n)\in CRPs} \left(\hat{n}(\vec{w}) - n\right)^2$$

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Machine Learning and Side Channels

- Use the following gradient in the optimization of ***w***:

$$\nabla_{\vec{w}_i} l = \sum_{(C,n)\in CRPs} 2(\hat{n}-n)\,\sigma(\vec{w}_i^T \varphi_i)(1-\sigma(\vec{w}_i^T \varphi_i))\,\varphi_i$$

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- In each summand, only terms with index „**i**“ appear…

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- This leads to a strong ***(exponential!)*** efficiency improvement

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Attack Results on Silicon CRP Data (from FPGAs)

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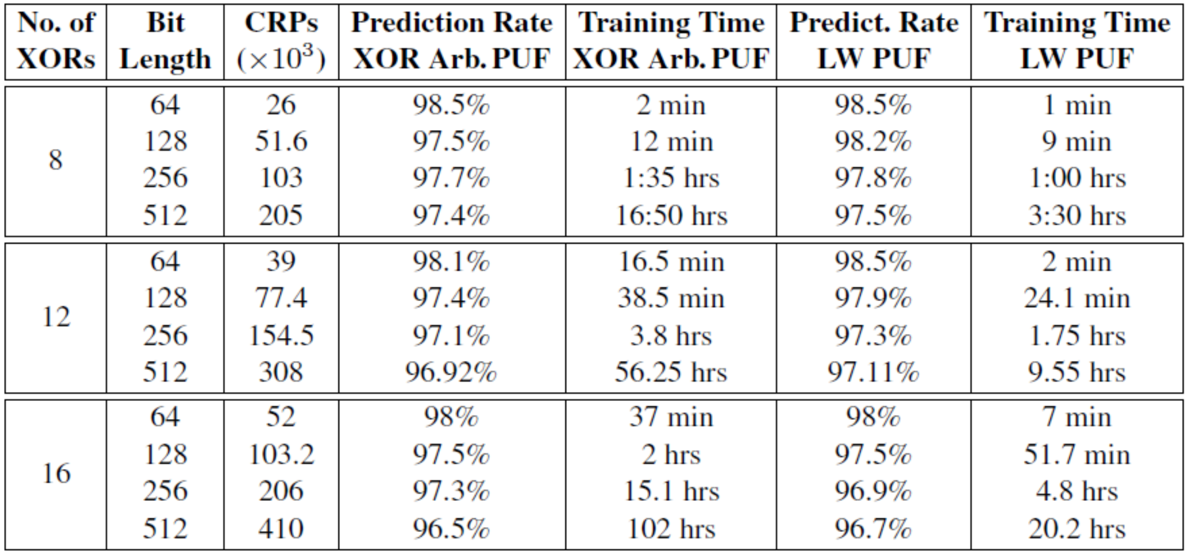

No. of XORs	Bit Length	CRPs ($\times 10^3$)	Prediction Rate XOR Arb. PUF	Training Time XOR Arb. PUF	Predict. Rate LW PUF	Training Time LW PUF
8	64	26	98.5%	2 min	98.5%	1 min
	128	51.6	97.5%	12 min	98.2%	9 min
	256	103	97.7%	1:35 hrs	97.8%	1:00 hrs
	512	205	97.4%	16:50 hrs	97.5%	3:30 hrs
12	64	39	98.1%	16.5 min	98.5%	2 min
	128	77.4	97.4%	38.5 min	97.9%	24.1 min
	256	154.5	97.1%	3.8 hrs	97.3%	1.75 hrs
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16	64	52	98%	37 min	98%	7 min
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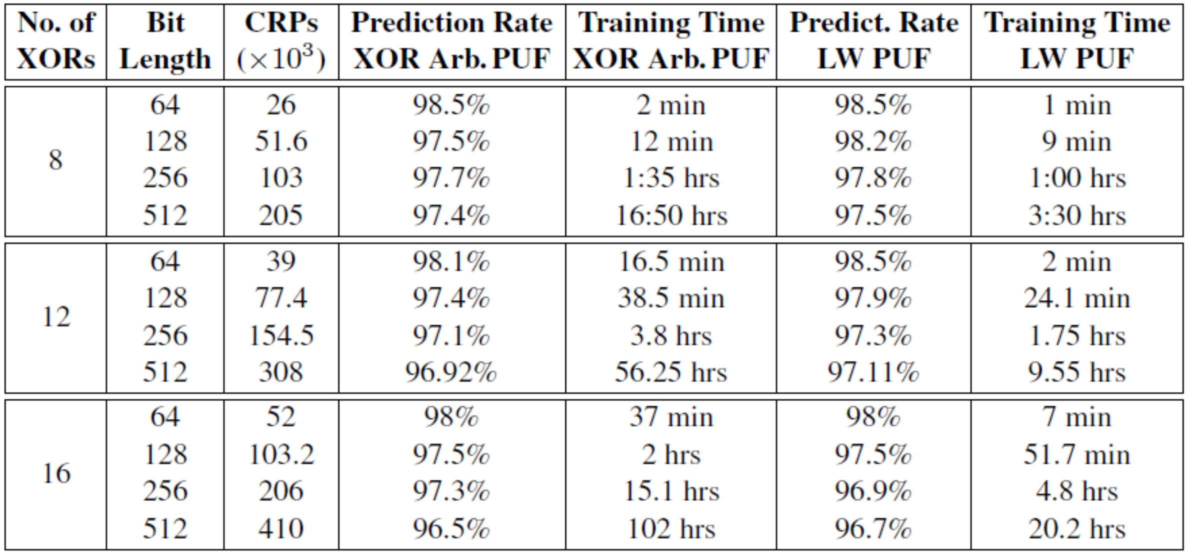

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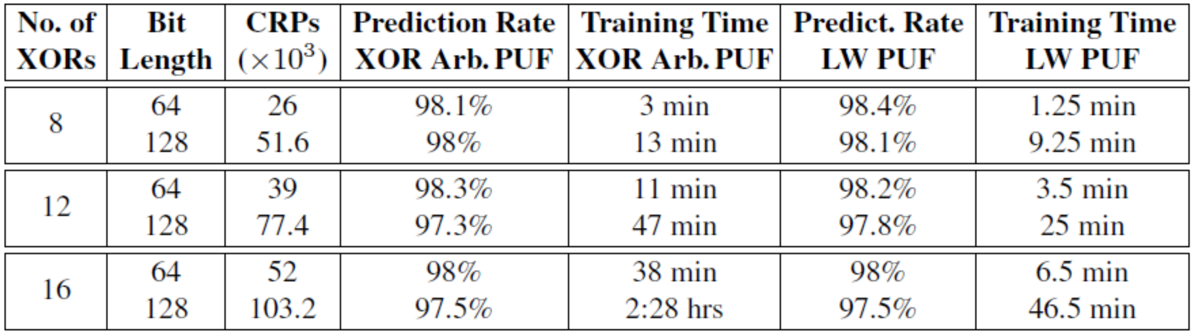

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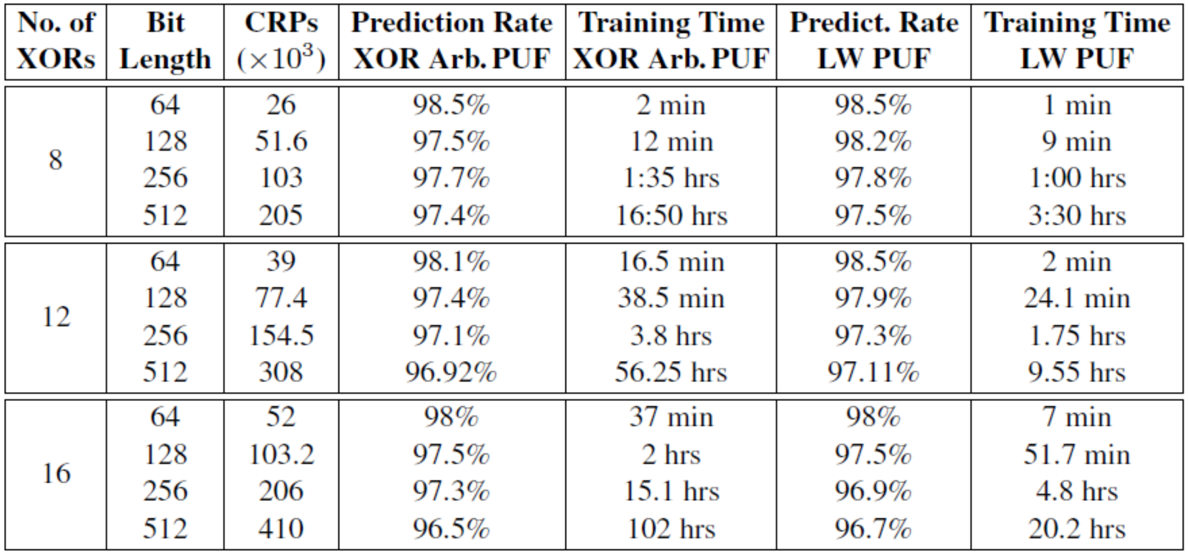

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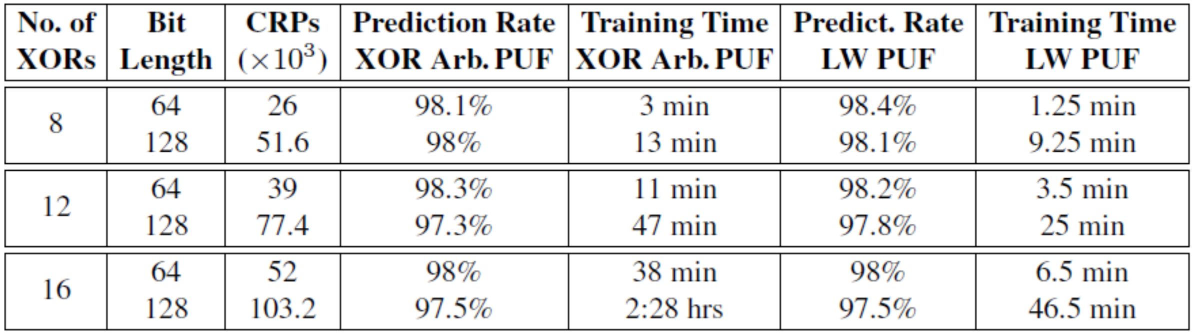

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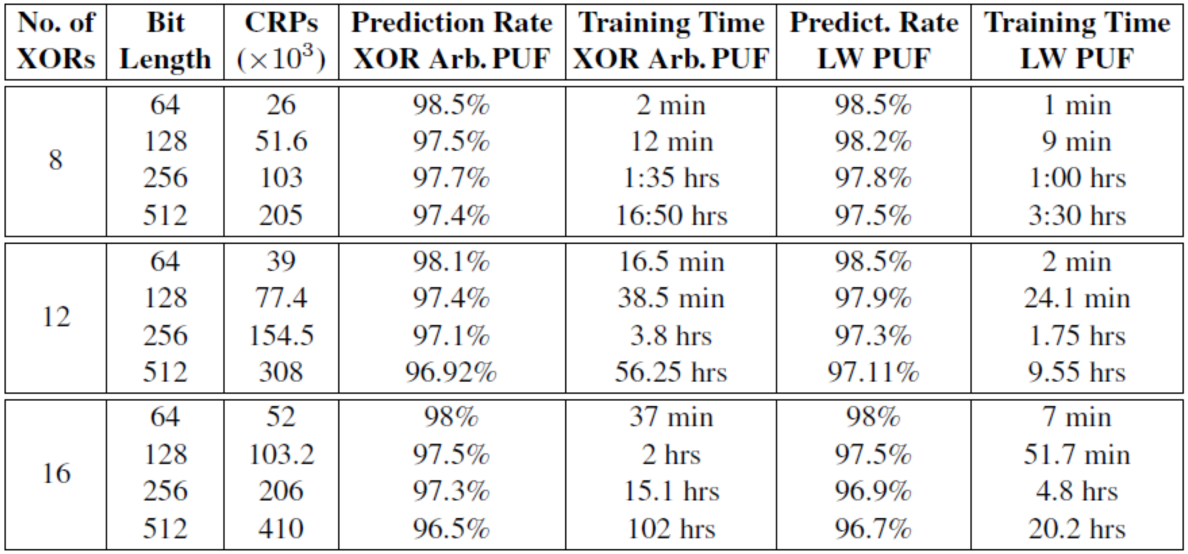

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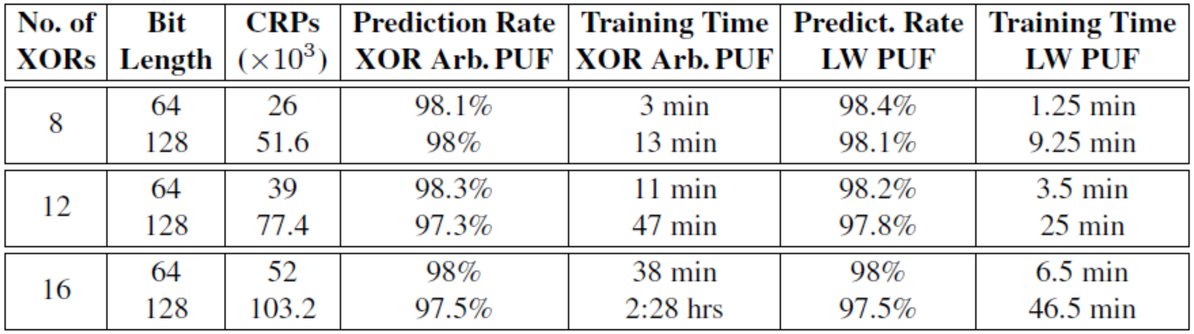

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Recall: *8 XORs had explicitly been suggested as secure…*

Asymptotic Performance Analysis on Simulated CRP Data

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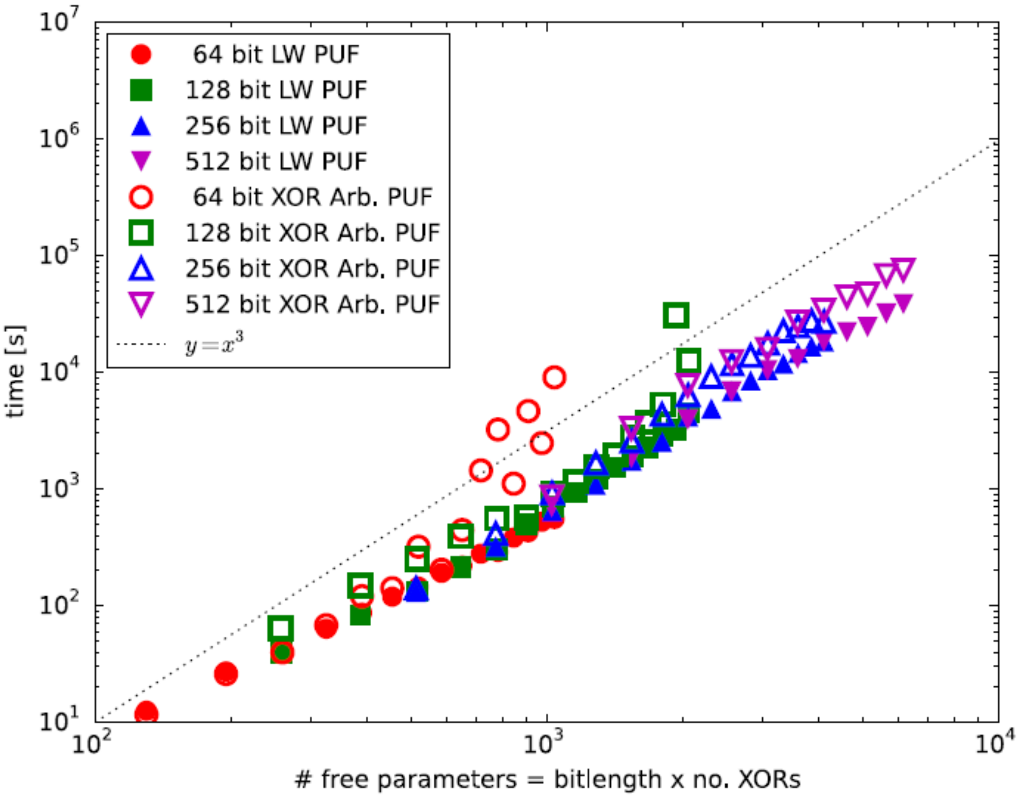

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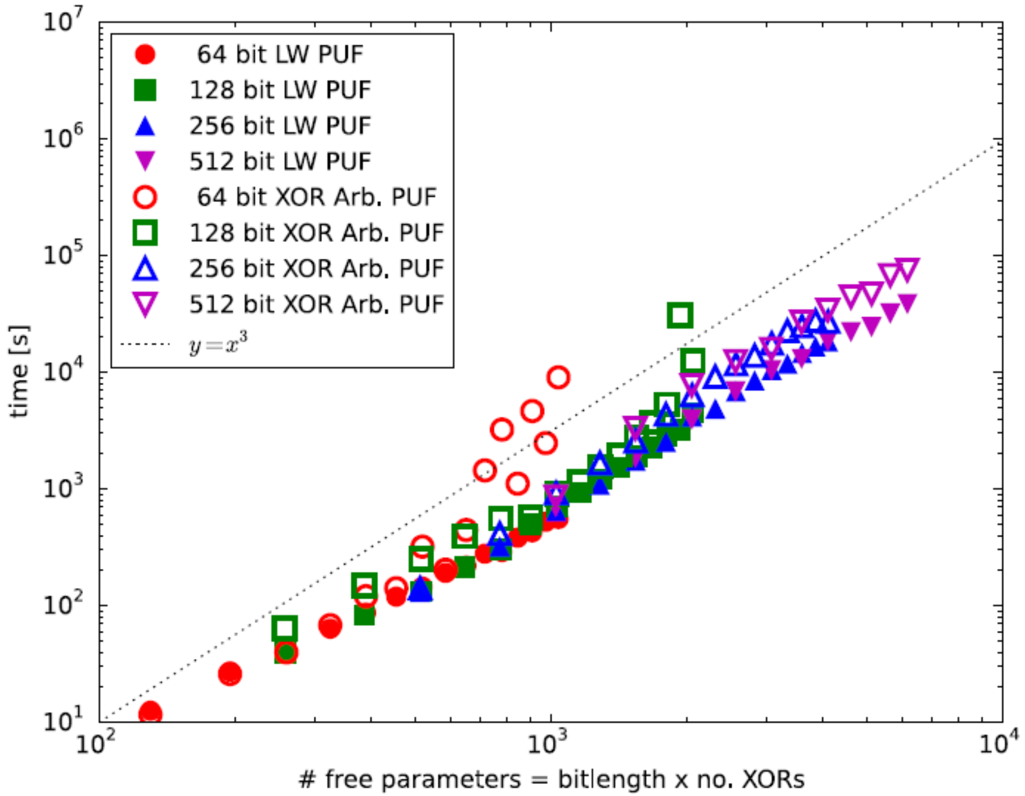

- Only ***cubic*** runtime and ***linear*** no. of CRPs required!
  - ***Compare:*** *Quadratic* runtime complexity and *linear* no. of CRPs of pure modeling attacks on **standard Arb PUFs** (i.e., without XORs)

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    that can notably **increase** attack performance (compare (1,2,3))
- Enables low-degree polynomial attacks for
  LW PUFs and XOR Arbiter PUFs
  - These were considered the most secure members
    of the Arbiter PUF family prior to our attacks
  - Only ***linear*** no. of CRPs and ***cubic*** runtime required

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- ***Watch this space, there‘s more to come!*** ☺