Fast Exhaustive Search for Polynomial Systems in $\mathbb{F}_2$

GPUs for Brute-Force Enumeration

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Outline

1 Executive Summary

2 Theory
   • About the Gray Code Method
   • Trade-offs

3 Empirical Side
   • On Commodity PCs
   • GPU Implementation

4 Discussion
Our Results

The Problem

Solve for \( n \) variables in \( \mathbb{F}_2 \) from \( m \geq n \) “generic” equations of low degree.

The Results: Generalized Gray Code Enumeration

- Data for 48 vars and 48 to 64 equations below, with estimate in USD to solve a Patarin IP challenge (64-64, quartic) in 1 month.
- Beat all Gröbner Bases solvers for practical sizes, generic case.

<table>
<thead>
<tr>
<th>Time (minutes)</th>
<th>Testing platform</th>
</tr>
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<tbody>
<tr>
<td>( d = 2 )</td>
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<td>( d = 3 )</td>
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</table>

B.-Y. Yang et al (IIS-TWISC@Sinica) Brute-Forcing \( \mathbb{F}_2 \) Polynomial Systems Aug. 18, 2010 3 / 24
Exhaustive Search in degree $d \geq 2$ – Summary

1. Complexity of each iteration: $\binom{n}{d} \rightarrow O(d \lg^\beta(d) \ n)$
2. Internal state: $1 \rightarrow \binom{n}{d-1}$

Headline (for all degree $d \geq 2$)

Exhaustive search requires $d$ XOR per candidate vector.

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Exhaustive search requires $d$ XOR per candidate vector.

3. Easy to implement efficiently... (more on that later)

4. ...on GPUs too!
Naive Search for \( n \mathbb{F}_2 \)-vars in \( m \) eqs of degree-\( d \)?

A \( \text{deg} = d \) equation over \( \mathbb{F}_2 \) has \( \binom{n}{k} \) terms at degree \( k \) for \( k \leq d \).

- \( \approx m \binom{n}{d} \) bit operations (OPs) per input, naively.
- \( \approx 2 \binom{n}{d} \) OPs per input if we compute serially and early-abort
- If logical operations are \( w \)-wide, we can bit-slice to speed up \( \sim w \times \)

“Folklore” Gray Code Search

Define \( b_i(x) := \) index of the \( i \)-th non-zero bit in binary representation of \( x \) \((-1\) if no such), then standard Gray code: \( G(k) = G(k - 1) \oplus 2^{b_1(k)} \).

With \( e_i \) representing the unit vector in the \( i \)-th direction, define:

\[
d_i f(x) := f(x + e_i) - f(x),
\]

then identifying a codeword \( x \) with a vector in \((\mathbb{F}_2)^n\), we have

\[
f(G(k)) = f(G(k - 1)) + d_{b_1(k)} f(G(k - 1)).
\]

When \( f \) quadratic: differentials \( d_i f \)’s affine, can evaluate in time \( O(n) \).

Per-input time complexity down to \( O(n) \), no change in memory use.
Recursive Gray Code Search

- Every 2 iterations $x_0$ (lowest bit of Gray Code) flips.
Recursive Gray Code Search

- It always goes: flip $x_0$, flip some other $x_i$, flip $x_0$.
- Hence, each time $x_0$ is flipped, the partial derivative to $x_0$ has last been seen (evaluated) at an input 1 bit away.
Recursive Gray Code Search

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- Hence, each time $x_0$ is flipped, the partial derivative to $x_0$ has last been seen (evaluated) at an input 1 bit away.
- $x_i$ (not low bit) always changes when the $i$ bits below $= 10 \cdots 0$, and if we strike out the last $i$ bits of a Gray Code sequence, we get Gray Code with each entry repeated $2^i$ times, and $x_i$ as new low bit.
- Hence any differential w.r.t. $x_i$ also last evaluated 1 bit away.
- Mathematical Induction pushes this to any higher degree.
Recursive Gray Code Search

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- Hence any differential w.r.t. \( x_i \) also last evaluated 1 bit away.
- Mathematical Induction pushes this to any higher degree.

### Quadratic Example (with \( d_{ij}f(x) := d_i f(x + e_j) - d_i f(x) \))

\[
\begin{align*}
    f(1) - f(0) & = d_0 f(0) \\
    f(11) - f(1) & = d_1 f(1) = d_1 f(0) + d_{01} \\
    f(10) - f(11) & = d_0 f(11) = d_0 f(10) = d_0 f(0) + d_{01} \\
    f(110) - f(10) & = d_2 f(10) = d_2 f(0) + d_{12} \\
    f(111) - f(110) & = d_0 f(111) = d_0 f(11) + d_{02} \\
    2 \text{ XORs/input} & = \ldots (n/2) \times \text{speedup, } n \times \text{RAM use}
\end{align*}
\]
Part of 5-bit Gray Code Example Table

Note that the initial appearance of each δ requires a setup.

<table>
<thead>
<tr>
<th>index</th>
<th>code</th>
<th>$b_1$</th>
<th>$b_2$</th>
<th>$b_3$</th>
<th>$b_4$</th>
<th>actions (quadratic)</th>
<th>actions (quartic)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>00000</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>δ += δ₀</td>
<td>δ += δ₀</td>
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<tr>
<td>00001</td>
<td>00001</td>
<td>0</td>
<td>-1</td>
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<td>-1</td>
<td>δ += δ₁</td>
<td>δ += δ₁</td>
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<tr>
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<td>1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>δ += (δ₀ += C₀,₁)</td>
<td>δ += (δ₀ += δ₀,₁)</td>
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<tr>
<td>00100</td>
<td>00110</td>
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<td>δ += δ₂</td>
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</tr>
</tbody>
</table>

Initialization Costs

When $i_1 > i_2 > \cdots > i_k$, the differential $d_{i_1, i_2, \ldots, i_k}$ appears initially as

$$\frac{\partial^k}{\partial x_{i_1} \partial x_{i_2} \cdots \partial x_{i_k}} f(e_{i_1-1} + e_{i_2-1} + \cdots + e_{i_k-1})$$

sum of $\sum_{j=0}^{d-k} \binom{k}{j}$ coefficients total $\approx \binom{n}{d-1} d$ XORs.
Partial \((s\text{-of-}n)\) Evaluation

Substituting \(s\) variables out of \(n\) to get \(2^s\) subsystems in \(n - s\) variables.
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Why Do We Need Partial Evaluation

- Required for Parallel Processing
- Convenient for memory management
- Optimization (for Enumeration and Check)
**Partial (s-of-n) Evaluation**

Substituting $s$ variables out of $n$ to get $2^s$ subsystems in $n - s$ variables.

### Why Do We Need Partial Evaluation

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### Things to Note

- Coeffs of deg-$k$ terms are deg $= d - k$ poly in the $s$ vars.
- Highest order coefficients are constant, can be shared.
- Store coefficients of subsystems out to buffer DRAM, may require two-stages if memory is limited (e.g., GPUs).
- Basically same code as for enumeration
Early Abort and Architectural Concerns

- Machine test-for-0 on $w$-bit-wide word, does $w$ ANDs + branch.
- Evaluating many eqs. wastes less than not using machine instructions.
- So “enumerate” on $f(0) \ldots f(w-1)$ then “check” $2^{n-w}$ passers.
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Complete Granularity: Enumeration and Partial Eval as One?

\[
V^{(i)} := \{ x \in \{0, 1\}^n : f^{(0)}(x) = f^{(1)}(x) = \ldots = f^{(i-1)}(x) = 0 \}
\]

To compute \( V^{(i)} \) from \( V^{(i-1)} \) for each \( i \)

Step 1.
- partial evaluate \( f^{(i)} \) with suitable \( s_i \)

Step 2.
- evaluate \( f^{(i)}(v) \) by substituting \( v \in V^{(i-1)} \) into the corresponding subsystem

If components of \( f(x) = 0 \) are filters, what is the best \#vars to partially evaluate from the equation \( f^{(i)} \)?
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**Complete Granularity: Enumeration and Partial Eval as One?**

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**To compute $V^{(i)}$ from $V^{(i-1)}$ for each $i$**

**Step 1.**
- **Partial evaluate** $f^{(i)}$
- **With suitable** $s_i$

**Step 2.**
- **Evaluate** $f^{(i)}(v)$ by substituting $v \in V^{(i-1)}$
- **Into the corresponding subsystem**

If components of $f(x) = 0$ are filters, what is the best #vars to partially evaluate from the equation $f^{(i)}$?

Needs $\left( 2 \cdot \sum_{j=0}^{d} \binom{n-s}{j} \right)$ times $2^{n-s}$ in $V^{(i)}$.

Plus must partial evaluate $2^s$ times $\sum_{j=0}^{d} (n-j) \binom{n-s}{j}$

$(n, n, n-1, \ldots, 0, \ldots)$

is generally good if we search for some good $s_i$. 
Early Abort and Architectural Concerns

- Machine test-for-0 on \( w \)-bit-wide word, does \( w \) ANDs + branch.
- Evaluating many eqs. wastes less than not using machine instructions.
- So “enumerate” on \( f(0) \ldots f(w-1) \) then “check” \( 2^{n-w} \) passers.

Complete Granularity: Enumeration and Partial Eval as One?

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“optimal” is \( (n, n, n-\ell, n-\ell-1, \ldots, h+1, h, 0, \ldots, 0) \) for small \( (h, \ell) \).
Check vs Enumerate

Changing check width

If per-input cost to enumerate is $c$, cost to check (verify) $v$, width $w$, and we want to change the width to $w' < w$, then we must check

$$c + 2^{-w} v > c' + 2^{-w'} v'$$

if $w' < w$, it simplifies to checking $c - c' > 2^{-w'} v'$. 
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CPU with SSE2 instructions: Optimal Width=16

With SSE2, all widths are powers of two. Assuming that $w' = w/2$ and $c' \approx c/2$, then it is better to use $w'$-wide if $v' < 2^{w'}c'$.
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Since $2^{10} < v'/c' < 2^{14}$ in all cases, this points to our checking $w' = 16$ equations at a time being better than either 32 or 8.
Our Programs

Three Stages

- Partial Evaluation: at least partly done on the CPU.
- Enumerate: this accounts for more than 90% of runtime.
- Checking: always done on the CPU.

Code Generation

We have perl scripts that generate the programs given some parameters, which are very regular and straight-line code, for both GPU and CPU. These generated programs also capture our ideas about memory space allocation and register spilling, etc.
The SSE2 Instruction Set

- SSE2 instruction let you act in parallel on 8-, 16-, 32-, or 64-bit chunks simultaneously. Here we do 8 chunks at a time.
- Turns out that more than SSE2 instruction set does not help much.
- Intel Core’s can dispatch 3 operations on XMM registers per cycle, AMD CPUs only 2.
- Since we are working with more than 1 entries in an XMM register, it takes extra work to extract, particularly the PMOVMSKB instruction.
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Notes

- Branches are relatively cheap, so we use them instead of conditionals.
- $s$ is smaller than for GPUs since we do not need as many threads.
- But for both CPUs and GPUs, $s$ increase roughly linear as $n$. 
Performance Testing on PCs

Timing (mins) and Cycle counts at \( n = 48, \ m = 64 \)

<table>
<thead>
<tr>
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<td>0.70</td>
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Notes

- Cycle count is almost strictly a function of arch
- scaling with any modern core is almost perfect
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#### Notes
- Cycle count is almost strictly a function of arch
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C Intrinsics Code

```c
... 
diff0 ^= deg2_block[1];
res ^= diff0;
Mask = _mm_cmpeq_epi16(res, zero);
mask = _mm_movemask_epi8(Mask);
if(mask) check(mask, idx, x^155);
... 
```
C Intrinsics Code

...  
diff0 ^= deg2_block[ 1 ];  
res ^= diff0;  
Mask = _mm_cmpeq_epi16(res, zero);  
mask = _mm_movemask_epi8(Mask);  
if(mask) check(mask, idx, x^155);  
...

Assembly Code

.L746:
    movq 976(%rsp), %rax //  
    pxor (%rax), %xmm2 // d_y ^= C_yz  
    pxor %xmm2, %xmm1 // res ^= d_y  
    pxor %xmm0, %xmm0 //  
    pcmpeqw %xmm1, %xmm0 // cmp words for eq  
    pmovmskb %xmm0, % eax // movemask  
    testw %ax, %ax // set flag for branch  
    jne .L1266 // if needed, check and
.L747: // comes back here
Performance Analysis

Instruction counts

- For quadratics 2 XORs, then 1 COMPARE, then a PMOVMSKB, then a test-and-branch. Hence, 6 instructions including 3 XMM loads. Ideal value is 3 cycles/loop. Actual value is slightly higher.
- For cubics/quartics, 7/8 XMM instructions respectively.
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Comparison to PS3

Version used for cryptanalysis is sold at a subsidy (US$300)
- 6 × 3.2GHz synergetic processing elements (SPEs) usable,
- each SPE does 128-bit wide logical OP/cycle in main pipeline,
- with a secondary pipeline to handle bookkeeping.

Hence max. 6 × 3.2GHz 128-bit OPs.
### Performance Analysis

#### Instruction counts
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#### Comparison to PS3
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#### The competition
- AMD K10+ can do 4 core × 2 = 8 XMM OPs/cycle.
- Intel Quad Core’s can do 4 core × 3 = 12 XMM OPs/cycle.
- The K10+ has utilization ratio ∼ 7/8, So a 3.2GHz Phenom IIx4 (or 2.66GHz Ci7) always beats a Cell.
nVidia G200 GPU on GeForce GTX 280 / Tesla C1060
470 mm², TDP: 204 watts (TSMC 55nm), >1.4 bil transistor, w. ≈ 1GB DRAM

1062.72 GFLOPS (single-precision), 159 GB/s mem bandwidth vs. 106.56 GFLOPS, 25.6 GB/s of Intel Core i7 at 3.33 GHz

- 30 “Multiprocessors” (MPs, Real Units of GPU Computing)
  - 8 ALUs, each can do 1 FMADD/cycle @ 1.296GHz
  - 2 Special Function Units, each 2 actions/cycle (incl. FMUL)
  - 16k registers (each 32bits), 16kB shared memory
  - 8kB constant cache into 64kB constant area
  - Latency: 22-26 cycles from SRAM 20 cycles, > 400 cycles from DRAM.
  - Opportunitistic but in-order dispatcher, 1 64-bit instruction decode per 4 cycles, ≥ 128 lightweight hardware threads (4 “warps”) needed for performance. We don’t even mention the Magic Textile Units.

- How to Program with CUDA
  - Program in C-like language *.cu file
  - Compile with nvcc to pseudomachine code (*.ptx).
  - Load with nVidia driver, load/launch from the main program.
  - Buggy compiler and can only jump to first 16k instructions (!).
The “if (X=0) Y=Z;” bit is actually the magic words to emit a predicated move, a 32-bit “half instruction”.

```c
... 
diff0 ^= deg2_block[ 3 ];  // d_y^=d_yz
res ^= diff0;            // res^=d_y
if( res == 0 ) y = z;    // cmov
if( res == 0 ) z = code233; // cmov
diff1 ^= deg2_block[ 4 ];
res ^= diff1;
if( res == 0 ) y = z;
if( res == 0 ) z = code234;
diff0 ^= deg2_block[ 0 ];
res ^= diff0;
if( res == 0 ) y = z;
if( res == 0 ) z = code235;
... 
```
2.6 SP cycles for quadratics

The inner loop has 5-6 instructions but < 3 cycles, clearly the SFU can dispatch some instructions, very well.

```
... 
xor.b32 $r19, $r19, c0[0x000c]    // d_y^=d_yz
xor.b32 $p1|$r20, $r17, $r20
mov.b32 $r3, $r1
mov.b32 $r1, s[$ofs1+0x0038]
xor.b32 $r4, $r4, c0[0x0010]
xor.b32 $p0|$r20, $r19, $r20    // res^=d_y
@$p1.eq mov.b32 $r3, $r1
@$p1.eq mov.b32 $r1, s[$ofs1+0x003c]
xor.b32 $r19, $r19, c0[0x0000]
xor.b32 $p1|$r20, $r4, $r20
@$p0.eq mov.b32 $r3, $r1        // cmov
@$p0.eq mov.b32 $r1, s[$ofs1+0x0040] // cmov
... 
```

Switching to predicated branch instead of predicated move makes each input take some 3.5 cycles on average!
Due to artifacts of GPU programming, threads return “no possible solution”, “one possible solution”, and “too many possible solutions”. The last is rerun completely on CPU.
CPU vs GPU
Need to rerun a thread

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**GPU Thread-Checking Probability**

If we have $n$ variables, pre-evaluate $s$, and check $w$ equations via Gray Code, then the probability of a subsystem with $2^{n-s}$ vectors including at least two candidates $\approx \binom{2^{n-s}}{2}(1 - 2^{-w})^{2^{n-s}}(2^{-w})^2 \approx 1/2^{2(s+w-n)+1}$, provided that $n < s + w$. 

Example
For $n = 48$, $s = 22$, $w = 32$, the thread-recheck probability is about 1 in $2^{13}$, and we must re-check about $2^9$ threads (using Gray Code).
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It gains little with conditionals (a packed SUBTRACT update a counter then 3 bookkeeping instructions, still 3 loads) over branching on CPU and a thread-check is expensive, hence the latter.
Performance Comparison at 32 variables, 64 equations

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Each MP with 8 ALUs (SPs) can potentially dispatch 8 instruction per cycle or more, but the DRAM controllers can only load once every cycle to each MP. Hence, we can have at most one DRAM load out of every 8 instructions ($< 12.5\%$) if we wish to get full use from ALUs.
GPU Memory Pressure Partly Explained

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For quartics (with parameters) we chose through empirical testing, some 23\% of instructions involve a DRAM operand, so throughput of an MP is at halved at least, and in fact, this is observed.
Summary

Take-Away Point

GPUs are good for cryptanalysis.
Summary

Take-Away Point
GPUs are good for cryptanalysis and easier than FPGAs.

Devil is in the Details
Easy to get “working”, but hard to get “just right”.

For not-too-overdetermined $F_2$ systems in the practical range, Brute Force works better than $F_4$ and other Gröbner basis solvers. This affects, for example, security guarantees of QUAD-type stream ciphers.

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A full version will be uploaded to the ePrint Archive prior to journal submission, and we may have packages for people to download and use.
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Credits

- This talk describes joint work with
  - Charles Bouillaguet, ENS, France
  - Adi Shamir, Weizmann Institute (visiting ENS)

- I am also joined by my conspirator Doug Cheng and kids from our lab
  - Tony (Tung) Chou, EE, Nat’l Taiwan U
  - Hsieh-Chung Isidore Chen, IIS, Academia Sinica
  - Ruben Niederhagen, IIS & TU Eindhoven

Also many thanks to Ming-Shing Chen for general support.
Questions or comments?