Trojan Side Channels

Lightweight Hardware Trojans through Side Channel Engineering

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University of Massachusetts Amherst

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Ruhr-Universität Bochum

CHES Workshop 2009

A Semiconductor Manufacturing Flow

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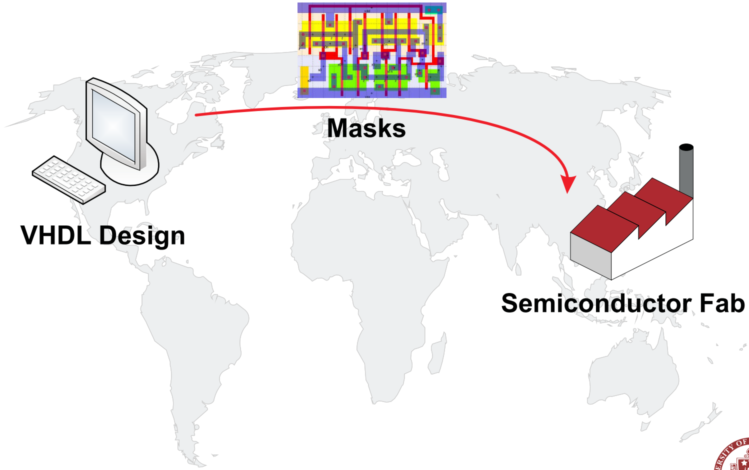

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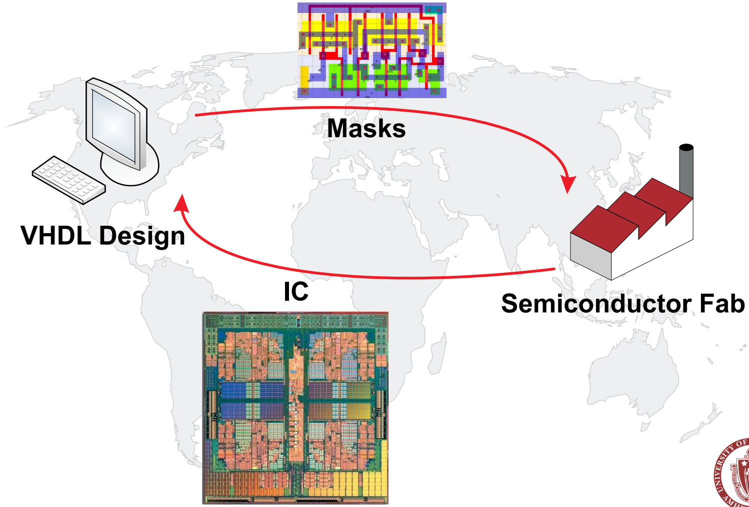

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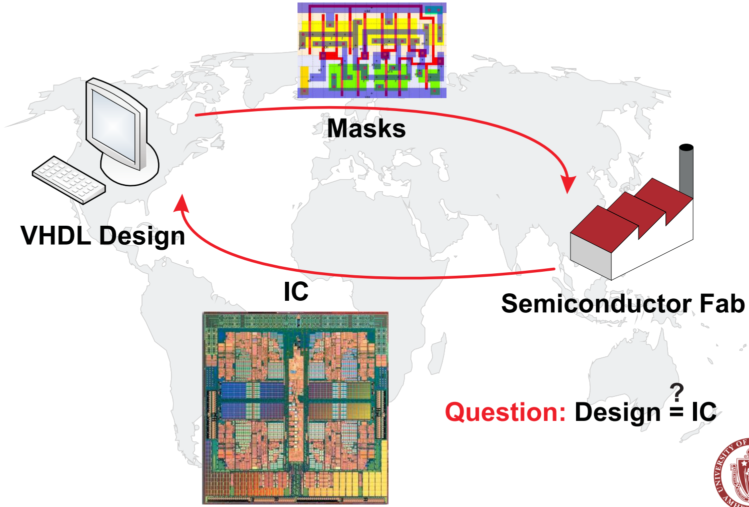
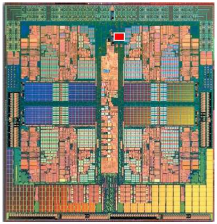


Question: Design $\overset{?}{=}$ IC

Trojan Hardware

Action: Functionality of the malicious hardware

- Modify functionality
- Leak secret information



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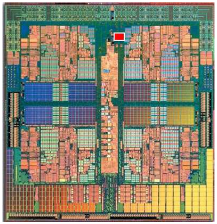
- "Always on"
- Triggered by timer/counter
- Event controlled
  - Sequence
  - State



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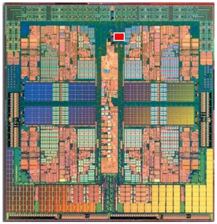

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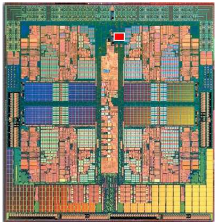

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- Via I/O pins
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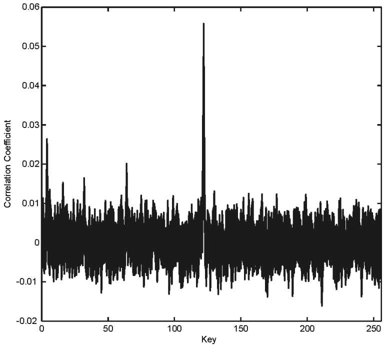
Combining two Concepts

Ingredients:

Side Channel Analysis



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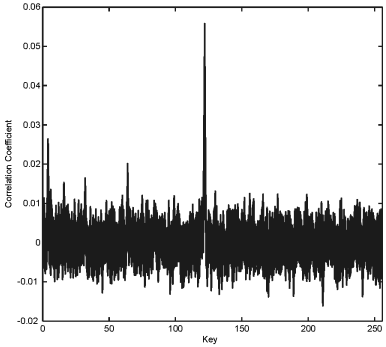

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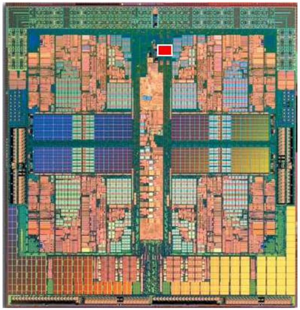
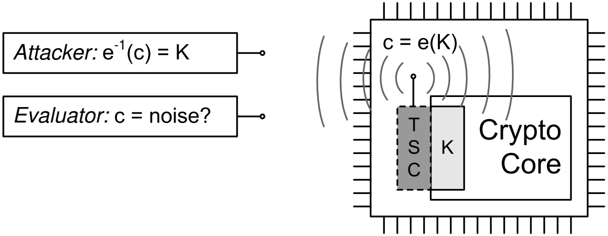


Our Model of an Trojan Side Channel Scenario



The Concept of Trojan Side Channels:

- Use subtle side-channels to leak information
  $\Rightarrow$ Replacing leakage via I/O pins

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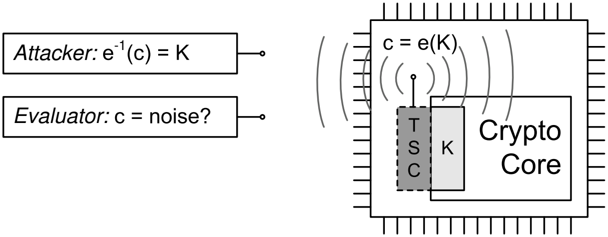

The Concept of Trojan Side Channels:

- Use subtle side-channels to leak information
  $\Rightarrow$ Replacing leakage via I/O pins
- "Encrypt" the Trojan
  $\Rightarrow$ Only the implementer may access the information

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- Target device uses reverse engineering countermeasures

How to Design a Trojan Side Channel

Resulting Design Goals

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Detectability:

- **Size:** Low gate count or parametric changes only
- **Side Channel Leakage:** Must not be detected by power analyses
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Usability:

Encryption property: TSC is only accessible by its implementer

Components of a Trojan Side Channel

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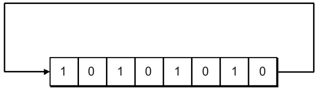
3. A leakage circuit

- Maps output of the combination function to physical leakage
- Can sometimes be realized within the combination function

The Leakage Circuit

For FPGAs:

- Look-up table as circular shift register
- Toggling flip-flops
- Other glitching logic
- ...



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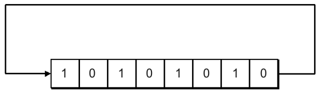

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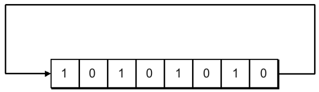

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But: More leakage makes detection easier for everyone

First Practical Results

We demonstrate two examples of Trojan Side Channels:

1. Spread Spectrum Trojan Side Channel

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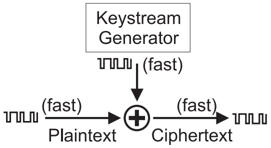
2. Input Modulated Trojan Side Channel

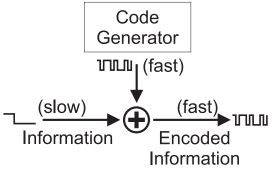
Spread Spectrum Theory on One Slide

Encoding: Very similar to a stream cipher

Stream Cipher:



CDMA Modulator:



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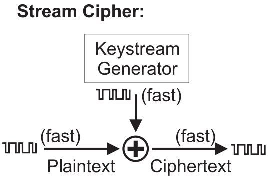
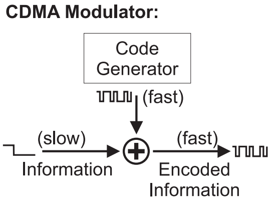
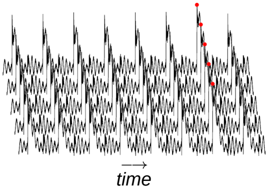
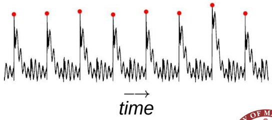


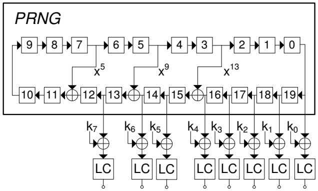


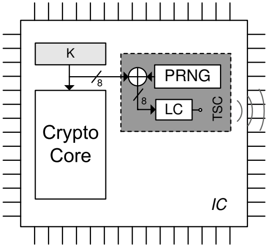
Decoding: Very similar to a correlation power analysis





Spread Spectrum TSC





Components:

Internal state: Introduced linear feedback shift register (LFSR)

Combination function: Bitwise XOR with LFSR outputs

Leakage circuit: 8 parallel flip-flops per bit

Encryption property: Unknown PRNG sequence

Detection of the CDMA TSC

Method to detect this kind of Trojan:

1. Use fixed key and average over many traces

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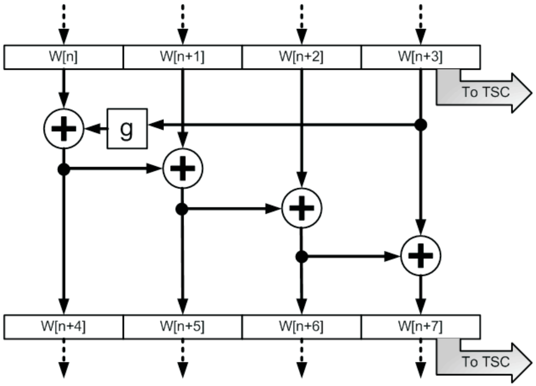
How to improve this TSC:

- Transfer only nonlinear combinations of bits (see second TSC)
- Use input to initialize the code generator

The Input Modulated Trojan Side Channel

Scenario:
TSC attached to AES-128 key schedule



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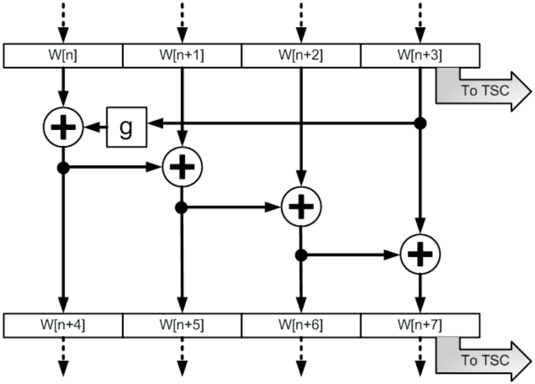
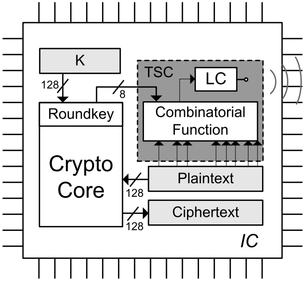


Background:
16 bits of the schedule sufficient to attack the key

The Input Modulated Trojan Side Channel

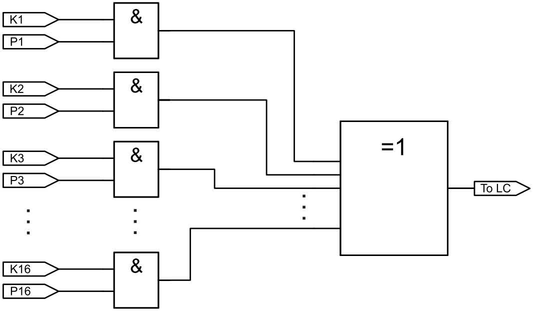


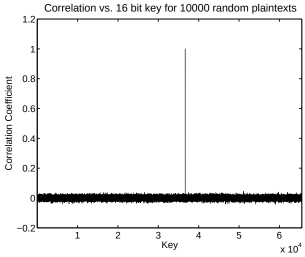
Components:

- Internal State: 16 bits of plaintext
- Combination Function: next slide
- Leakage Circuit: Look-up table as circular shift register

The Combination Function

Combination function used here:





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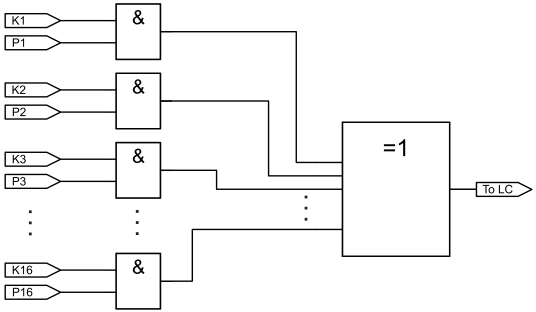

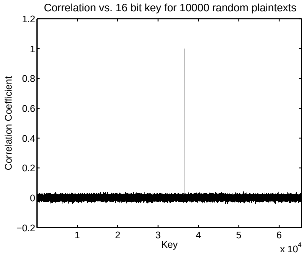

Design Criteria:

Good discrimination properties in DPAs

Uses only few input bits and logic gates

Leakage hard to detect during SCA evaluation

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Question:
Where is the encryption property?

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- The choice of used plaintext bits is not known
- Their order is also a secret
- $\approx 2^{55}$ possible choices for an 8 bit TSC
- $\approx 2^{110}$ possible choices for an 16 bit TSC

Experimental Setup

Implemented: AES key schedule with input modulated TSC

Side-channel Attack
Standard Evaluation BOard
SASEBO

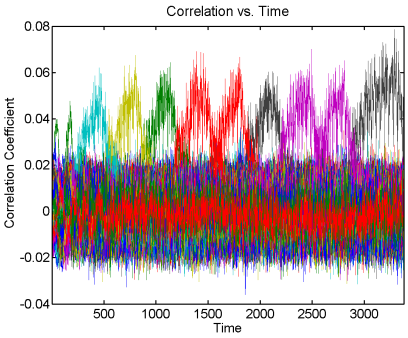
Device: Xilinx Virtex-2 PRO XC2VP7-5 FPGA @ 24MHz

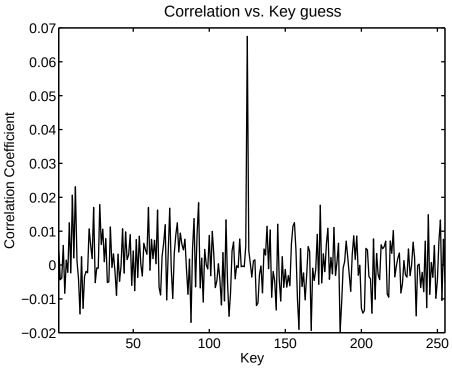
For more info on the SASEBO project:

Contact Akashi Satoh or visit the SASEBO website:

http://www.rcis.aist.go.jp/special/SASEBO/index-en.html

Experimental Results





Figures generated using 20.000 power traces

Summary

- New concept: Use side channels as building blocks
- Introduced the very flexible approach of Trojan Side Channels
- First practical results demonstrate feasibility of the concept

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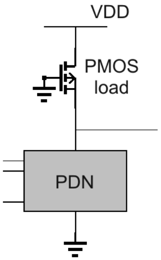
Thanks For Your Attention!

Any Questions?

The Leakage Circuit

For ASICs:

- Ratioed Logic
  - Pseudo-NMOS
  - Pseudo-PMOS
  - Other resistive load
- Precharge Logic (dynamic logic)
- ...



Note:
Gates don’t have to be sized to be functional, they only need to modify the power consumption!

Detection Methods

Four methods to detect malicious hardware:

1. Detection during regular testing (functional)

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   $\rightarrow$ Limited by the integrity of the additional logic

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- ASIC implementations
- TSCs with parametric modifications (like doping or geometry)