Accelerating AES with Vector Permute Instructions

Mike Hamburg

Stanford University

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Fast AES Implementations

- Lookup table for (MixColumns ∘ S-box)
- [DR '99, ..., BS '08]

- Vulnerable to cache-timing attacks
- Composite fields for hardware

[R '00, RDJKRR '02]

Bitslicing

- [B '97, ..., KS '09]
- ullet Very fast when encrypting \geq 8 blocks in parallel

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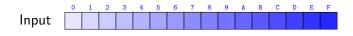
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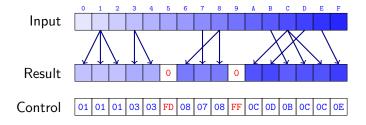
- [B '97, ..., KS '09]
- Very fast when encrypting \geq 8 blocks in parallel
- Today: composite fields and vector permutations
 - Fast even for only one block

Available on AltiVec, ARM NEON, SSSE3

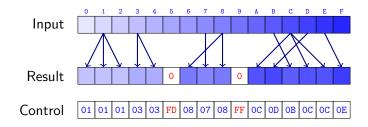


Control 01 01 01 03 03 FD 08 07 08 FF 0C 0D 0B 0C 0C 0E

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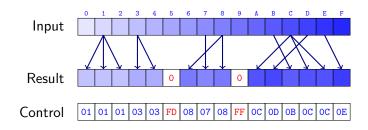


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- More powerful on AltiVec

Composite Fields

- ullet AES uses inversion over \mathbb{F}_{2^8}
 - Too complicated to compute directly

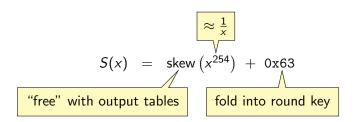
- Decompose \mathbb{F}_{2^8} as $\mathbb{F}_{2^4}[t]/(t^2+t+\zeta)$
 - 16 elements just right for vector permutes!

- Choice of basis is important!
 - We chose $(t, \overline{t} := t+1)$

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Computing $\frac{1}{xt+y\bar{t}}$ — Classical Inversion

Clear the denominator:

$$\frac{1}{xt + y\bar{t}} = \frac{x\bar{t} + yt}{xy + \zeta(x^2 + y^2)}$$

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- Needs log tables!
 - Not enough space on x86

• Multiply without multiplication:

$$\frac{xy}{x+y} = \frac{1}{\frac{1}{x} + \frac{1}{y}}$$

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$$\frac{xy + \zeta(x^2 + y^2)}{(1+\zeta)x + \zeta y} = \frac{1}{\frac{1}{x} + \frac{1}{\zeta(x+y)}} + y$$

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$$\frac{1}{xt + y\bar{t}} = \frac{t + \zeta}{\frac{1}{\frac{1}{y} + \frac{1}{\zeta(x+y)}} + x} + \frac{\bar{t} + \zeta}{\frac{1}{\frac{1}{x} + \frac{1}{\zeta(x+y)}} + y}$$

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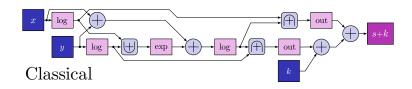
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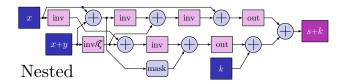
Multiply without multiplication:

$$\frac{1}{xt + y\bar{t}} = \frac{t + \zeta}{\frac{1}{\frac{1}{y} + \frac{1}{\zeta(x+y)}} + x} + \frac{\bar{t} + \zeta}{\frac{1}{\frac{1}{x} + \frac{1}{\zeta(x+y)}} + y}$$

- Not as bad as it looks!
- Division by zero a problem
 - Use "∞ bit"

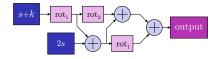
Computing $\frac{1}{xt+y\overline{t}}$ — Comparison





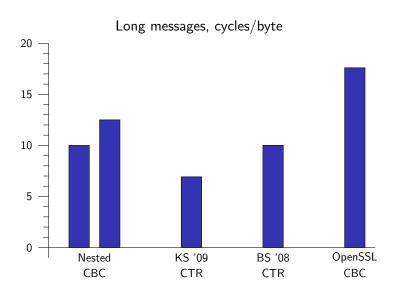
The Rest of the Cipher

- Don't compute ShiftRows
 - Fold into MixColumns permutations
- AddRoundKey before MixColumns
 - Modified key schedule
- MixColumns from s + k and 2s

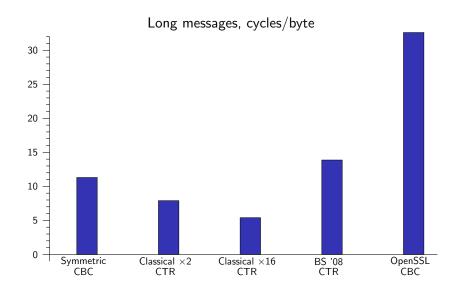


• Fold output basis shift into S-box

Performance – Nehalem



Performance – PowerPC G4e



Future Work

- Optimize more carefully for Intel
 - Up to 20% in microarchitectural tweaks
 - Up to 17% in CTR-mode caching
 - Byte-slicing?

- Implement other primitives
 - Camellia, LEX, Fugue, . . .

Package and distribute!

Fin

Questions?