

A New Side-Channel Attack on RSA Prime Generation

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Outline

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 - **r** Basic attack
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Facts (I)

- r Side-channel attacks on RSA implementations have a long tradition.
- r Nearly all of these attacks aim at the exponentiation with the private key. Only a few papers consider the key generation process (e.g., Clavier & Coron, 2006).



Facts (II)

If a smart card generates an RSA key outside the personalisation environment the key generation process may be vulnerable by side-channel attacks.



Side-channel attacks on RSA key generation

- Compared to side-channel attacks within the exponentiation phase the prospects for the attacker seem to be worse since
 - **r** the key is generated only once
 - r the generation process does not use any (known or chosen) external input
- r The type of the weaknesses and their exploitation may be different from side-channel attacks within the exponentiation phase.



Motivation

- r We present a side-channel attack on the RSA key generation process on a straight-forward implementation (proposed e.g. by Brandt et al. (1991), cf. also RSAREF toolkit)
- **r** The goal of our paper is two-fold, namely

r to demonstrate the fundamental vulnerability of the RSA key generation process against sidechannel attacks.

r to encourage the community to study the key generation process with regard to side-channel attacks

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Definition

$$r T = \{r_2 := 3, 5, 7, ..., r_N\}$$

/* trial base, consists of the first odd N-1 primes */



Prime generation algorithm (I)

1. Generate an odd (pseudo-) random number $v \in \{2^{k\text{-}1}\text{+}1, \, ..., 2^k\}$

2.

```
a) i := 2;
b) while (i \leq N) do { /*trial divisions*/
if (r<sub>i</sub> divides v) then {
v := v+2;
GOTO Step 2a; }
i<sup>++</sup>;
}
```



Prime generation algorithm (II)

```
c) m := 1;
d) while (m \le t) do {
              /* t = max # of primality tests */
        apply the Miller-Rabin primality test to v;
        if the primality test fails then {
               v := v+2;
               GOTO Step 2a; }
               m++:
```

```
3. p:= v (resp., q := v)
```



Assumptions

- **r** Power analysis allows the attacker
 - r to identify for each prime candidate v after which trial division the while-loop has terminated
 - r whether a Miller-Rabin test has been applied.

NOTE: If all trial divisions need approximately the same run-time it suffices to identify the beginning of the while-loop 2b) or the incrementation step v := v+2.



Remark

- **r** We further assume that
 - **r** the RNG is strong

r the trial division itself and the Miller-Rabin tests are perfectly protected against side-channel attacks

r Otherwise, even stronger attacks may exist.



Basic attack (I)

- r Notation: $v_0 = v, v_1 = v_0 + 2, ..., v_m = v_0 + 2m := p$
- **r** Basic observation:
 - r For v_j loop 2b) terminates after trial division by r $r \Rightarrow v_j \equiv 0 \pmod{r}$ r ⇒ p = v_m = v_i + 2(m-j) ≡ 2(m-j) (mod r)



Basic attack (II)

r <u>Generation of p:</u> $S_p := \{2\} \cup \{ r \in T | \text{ for at least } v_j \text{ the algorithm}$ terminated after the division by r }

r The CRT gives $a_p \equiv p \pmod{s_p}$ with $s_p := \prod_{r \in S_p} r$, and finally

$$a_q \equiv q \equiv a_p^{-1} n \pmod{s_p}$$

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Basic attack (III)

r Analogously (observing the generation of q)

$$\mathbf{b}_{\mathbf{q}} \equiv \mathbf{q} \pmod{\mathbf{s}_{\mathbf{q}}}$$
 for $\mathbf{s}_{\mathbf{q}} := \prod_{r \in S_q} r$
and

$$\mathbf{b}_{\mathbf{p}} \equiv \mathbf{p} \equiv \mathbf{b}_{\mathbf{q}}^{-1} \mathbf{n} \pmod{\mathbf{s}_{\mathbf{q}}}$$

 $c_p \equiv p \pmod{s}, c_q \equiv q \pmod{s}$ with $s := lcm(s_p, s_q)$



Basic attack (IV)

 $r p = sx_p + c_p$, $q = sy_q + c_q$ for unknown integers x_p , y_q

r The pair (x_p, y_q) is a zero of the irreducible bivariate integer polynomial f: $Z \times Z \rightarrow Z$, $f(x,y) := sxy + c_p y + c_q x - t$ with t:= $(n-c_p c_q) / s$

r If $log_2(s) > k/2$ the LLL algorithm finds the pair (x_p, y_p) in time polynomial in k (k = bit length of p and q).



Empirical results

- r Simulations of the attack with Magma (≅ perfect measurements)
- **r** k = 512; LLL requires at least $log_2(s) > 256$
- **r** Trial bases: $T_1 = \{3,5,...,251\}, /* \text{ odd primes} < 2^8 */$ $T_2 = \{3,5,...,281\}, T_3 = \{3,5,...,349\}$

Success Probabilities (basic attack)

	<i>T</i> ₁	T_2	T_3
$Prob(log_2(s) > 256)$	0.118	0.188	0.283
$Prob(log_{2}(s) > 277)$	0.055	0.120	0.208



Remark

- r If $log_2(s) < k/2$ the LLL-algorithm will not find the zero (x_p, y_p) .
- **r** One may guess the remainder p (mod r_i) for some further primes $r_1',...,r_m'$ so that s' := $s \cdot r_1' \cdot \cdots r_m'$ is sufficiently large.
- **r** <u>Drawback</u>: In the worst case the LLL algorithm has to be applied to all $r_1' \cdots r_m'$ admissible candidates (c_p', c_q') for (p (mod s'), q (mod s'))



Refinements of the attack

By exploiting further side-channel information from

r the trial divisions

r the extended Euclidean algorithm (computation of d (mod (p-1)) and d (mod (q-1))

many candidates for c_p ' can be excluded.

<u>Remark:</u> For k=512 this provides about 10-15 bits additional information.



Experimental results (I)

r Sample implementation on an ATMEL ATmega microcontroller

rnd2r(); testdiv512 (v,3); testdiv512 (v,5); testdiv512 (v,7); incrnd (v); testdiv512 (v,3); incrnd (v); testdiv512 (v,3); testdiv512 (v,5);

/* generates a random number */ /* trial division by 3 */

/* increments v by 2 */



Experimental results (II)

- **r** <u>Notation:</u> $x_1, x_2, ..., x_N$: power consumption during the particular clock cycles
- r Goal: Find a characteristic sample that identifies a trial division or an incrementation step

$$\begin{array}{c} x_1, x_2, \dots, x_{t-1}, \begin{matrix} x_t, x_{t+1}, \dots, x_{t+M-1} \\ \downarrow & \downarrow \end{matrix}, \begin{matrix} x_{t+1}, \dots, x_{t+M-1} \\ \downarrow & \downarrow \end{matrix}, \begin{matrix} x_{t+1}, \dots, x_{t+M-1} \\ \downarrow & \downarrow \end{matrix}, \begin{matrix} x_{t+M}, \dots, x_N \\ \downarrow & \downarrow \end{matrix}$$



Experimental results (III)

r The similarity function

$$a_j = \frac{1}{M} \sum_{i=1}^{M} |x_{i+j} - y_i|$$
 for $j \in \{1, ..., N-M\}$

compares $(y_1, ..., y_M)$ with the power consumption subsequence $(x_{j+1}, ..., x_{j+M})$ for all shift parameters j.

To compensate random local effects we finally applied

 $b_i := min \{a_i, \dots, a_{i+F-1}\}$

/*minimum over a 'window'*/





low peaks: large similarity, high peaks: large dissimilarity r

r sample sequence within the first incrementation step low peaks = positions of incrementation steps



Possible countermeasure

r regular refreshment of the prime candidates v_j by updating some bytes (e.g., XORing 8 bytes of every 10th candidate v_j with random bytes)



Final remarks

- r We have demonstrated the power of a sidechannel attack on a straight-forward prime generation algorithm.
- Simulations yielded success probabilities of 10 – 15 %, and practical experiments verified that the above-mentioned assumptions are indeed realistic.
- r Moreover, this paper shall motivate the community to devote more attention to the key generation step.



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