

Shuffling Against Side-Channel Attacks: *a Comprehensive Study with Cautionary Note*



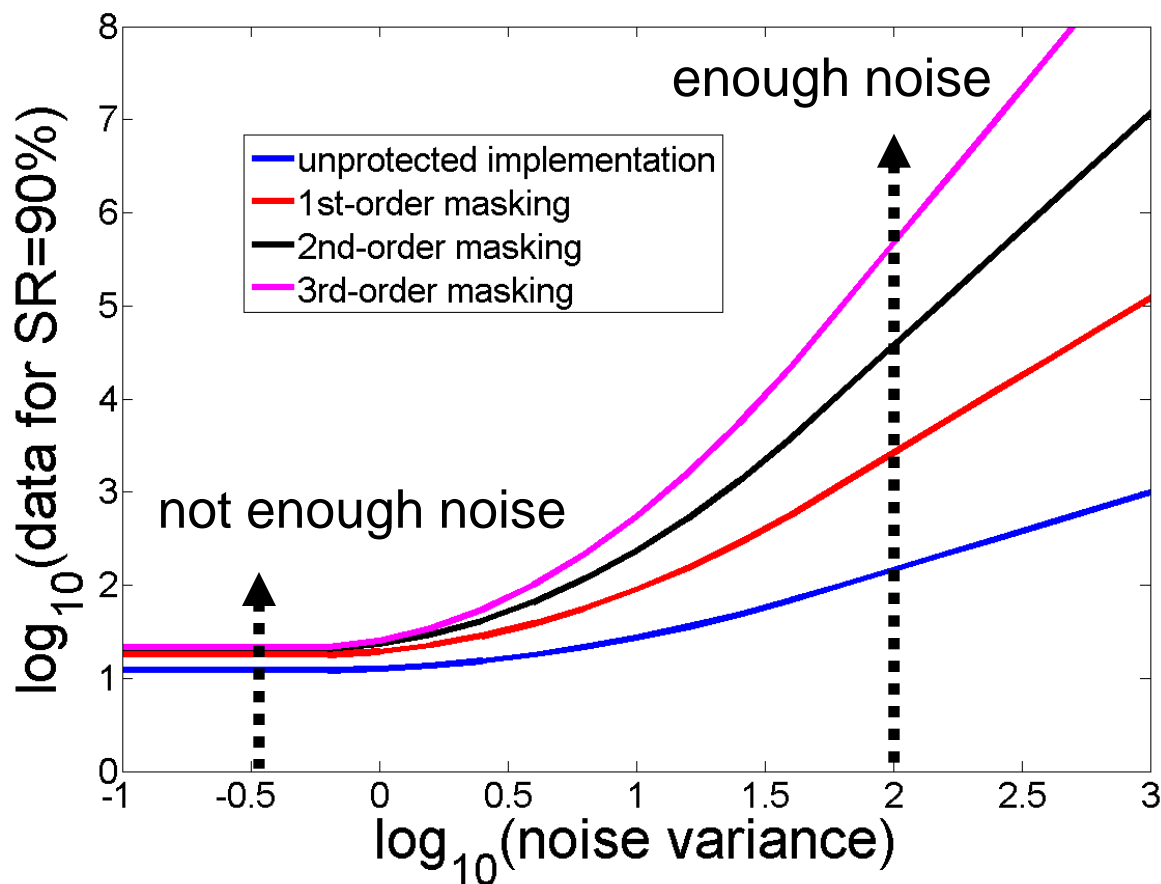
N. Veyrat-Charvillon, M. Medwed,
S. Kerckhof, ***F.-X. Standaert***

UCL Crypto Group, Belgium

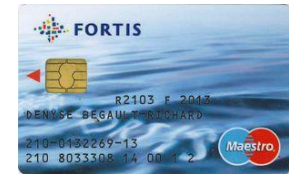
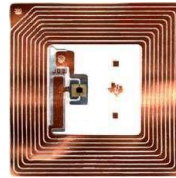
ASIACRYPT 2012, Beijing, China

- ASIACRYPT 2010: masking is an effective countermeasure against side-channel attacks

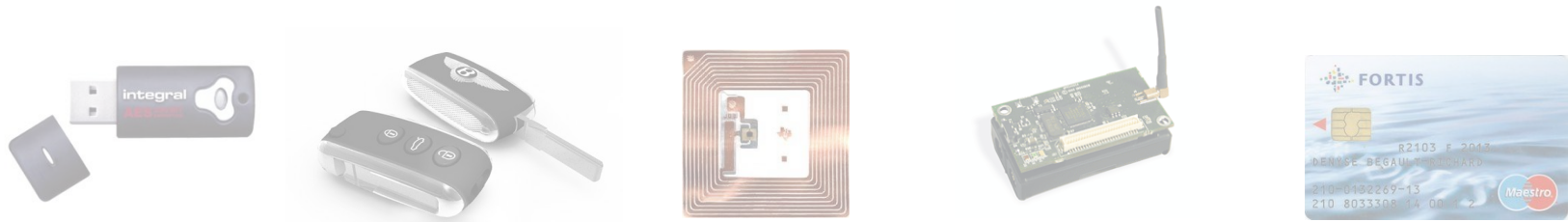
- ASIACRYPT 2010: masking is an effective countermeasure against side-channel attacks
 - *If there is sufficient measurement noise !!!*



- Problem: how to generate noise in small devices?

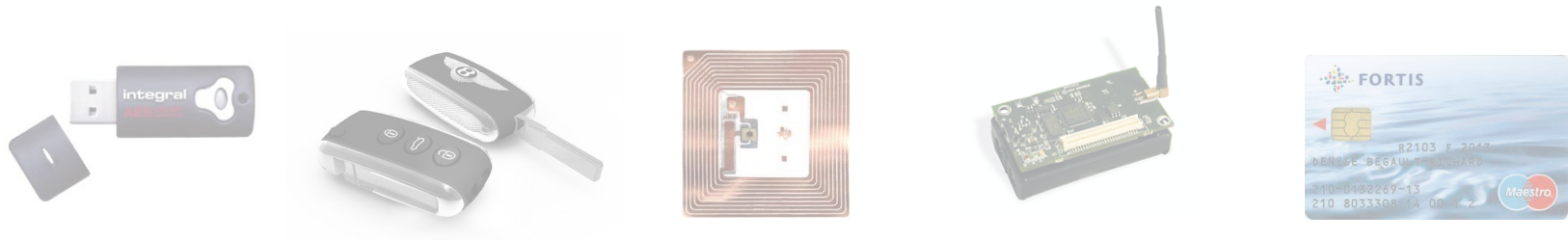


- Problem: how to generate noise in small devices?



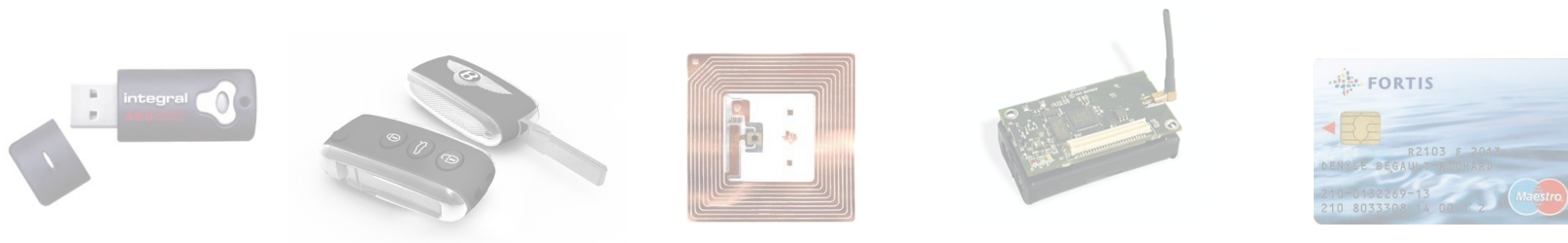
- Previous works: time randomization can help

- Problem: how to generate noise in small devices?



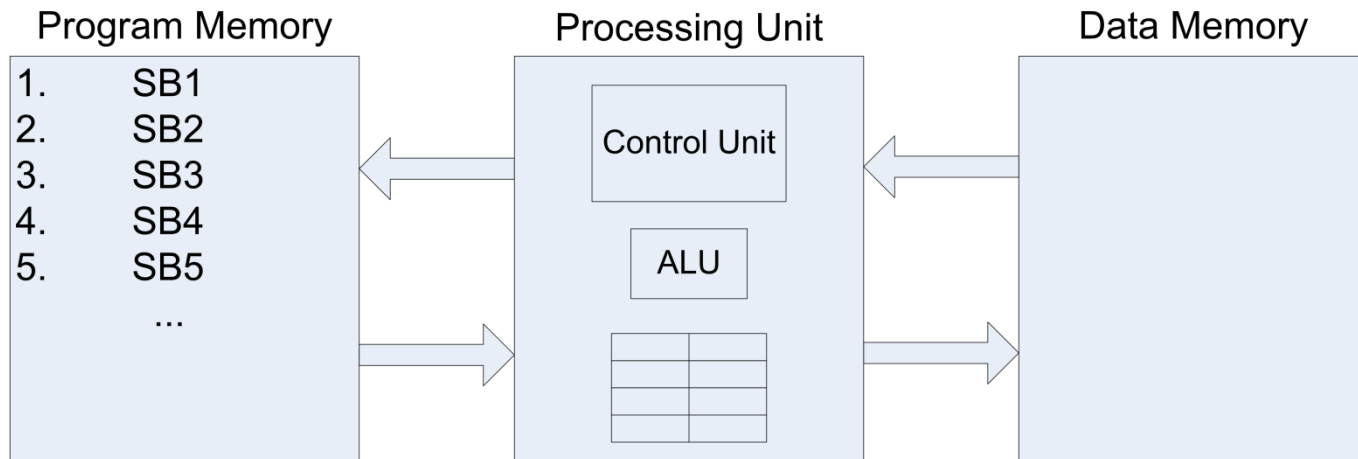
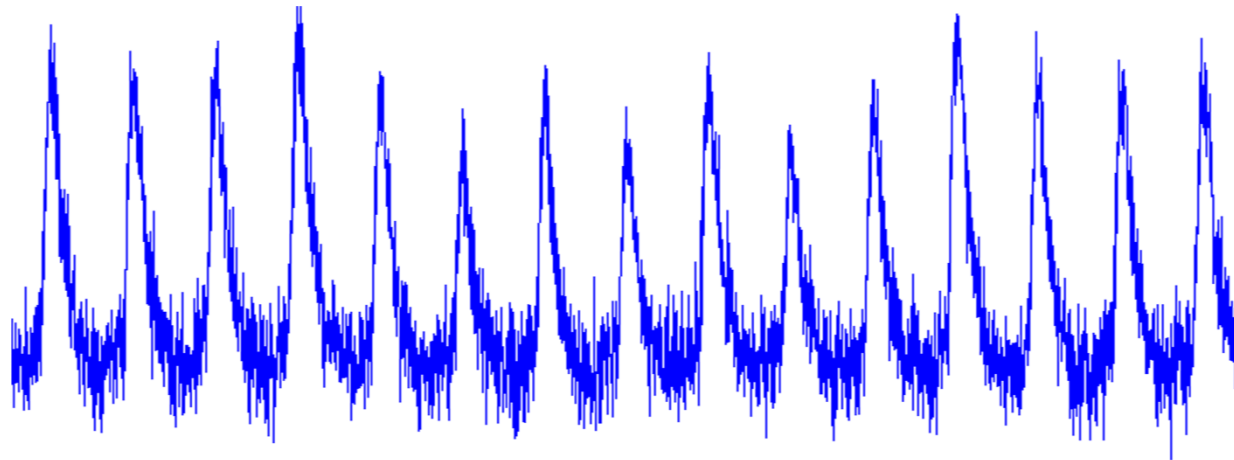
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- But we need to be careful with re-synchronization
 - e.g. random insertion of dummy operations is not enough [Durvaux et al./CARDIS2012]

- Problem: how to generate noise in small devices?

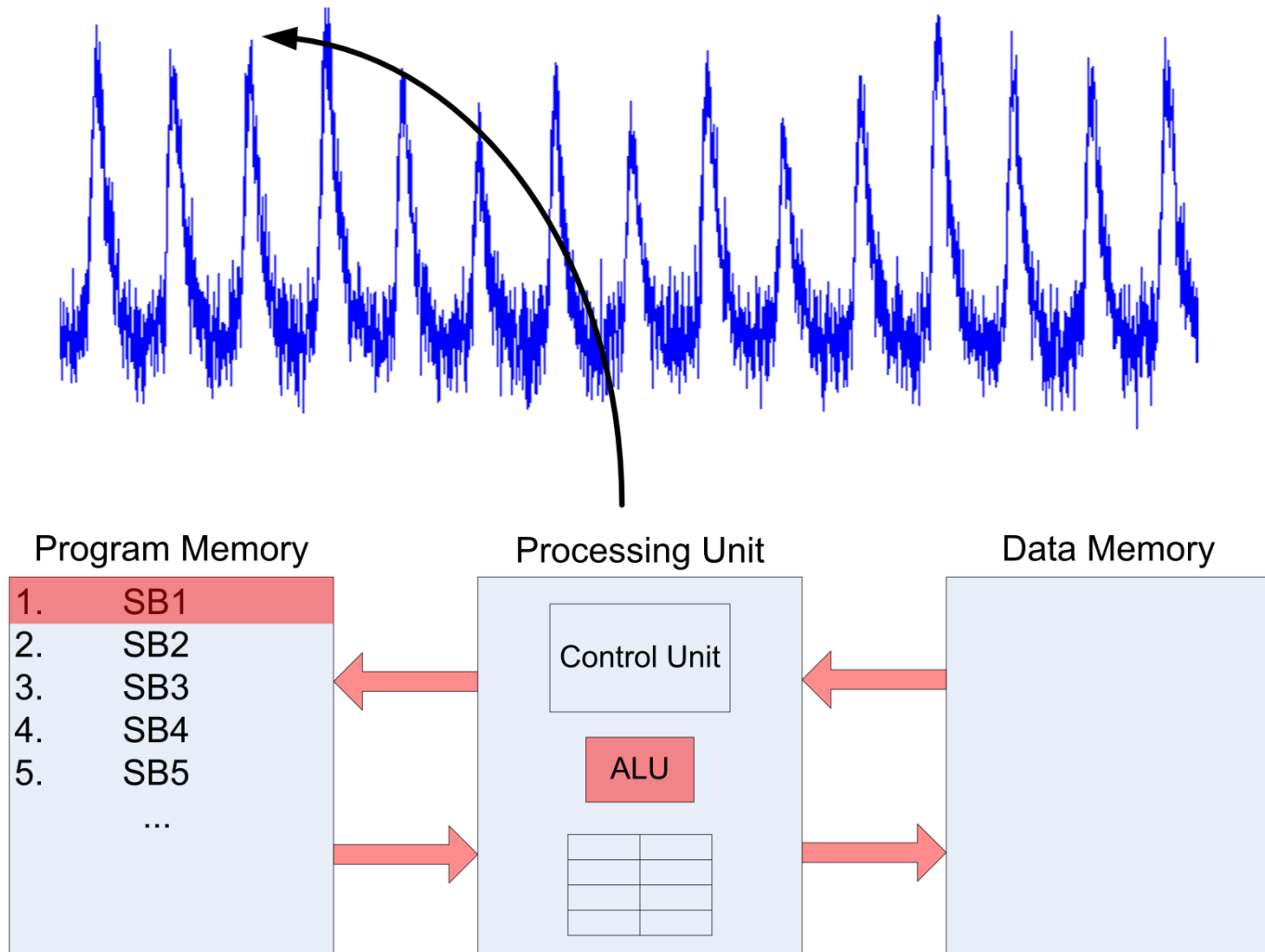


- Previous works: time randomization can help
- But we need to be careful with re-synchronization
 - e.g. random insertion of dummy operations is not enough [Durvaux et al./CARDIS2012]
- **Best known option so far: shuffling operations**

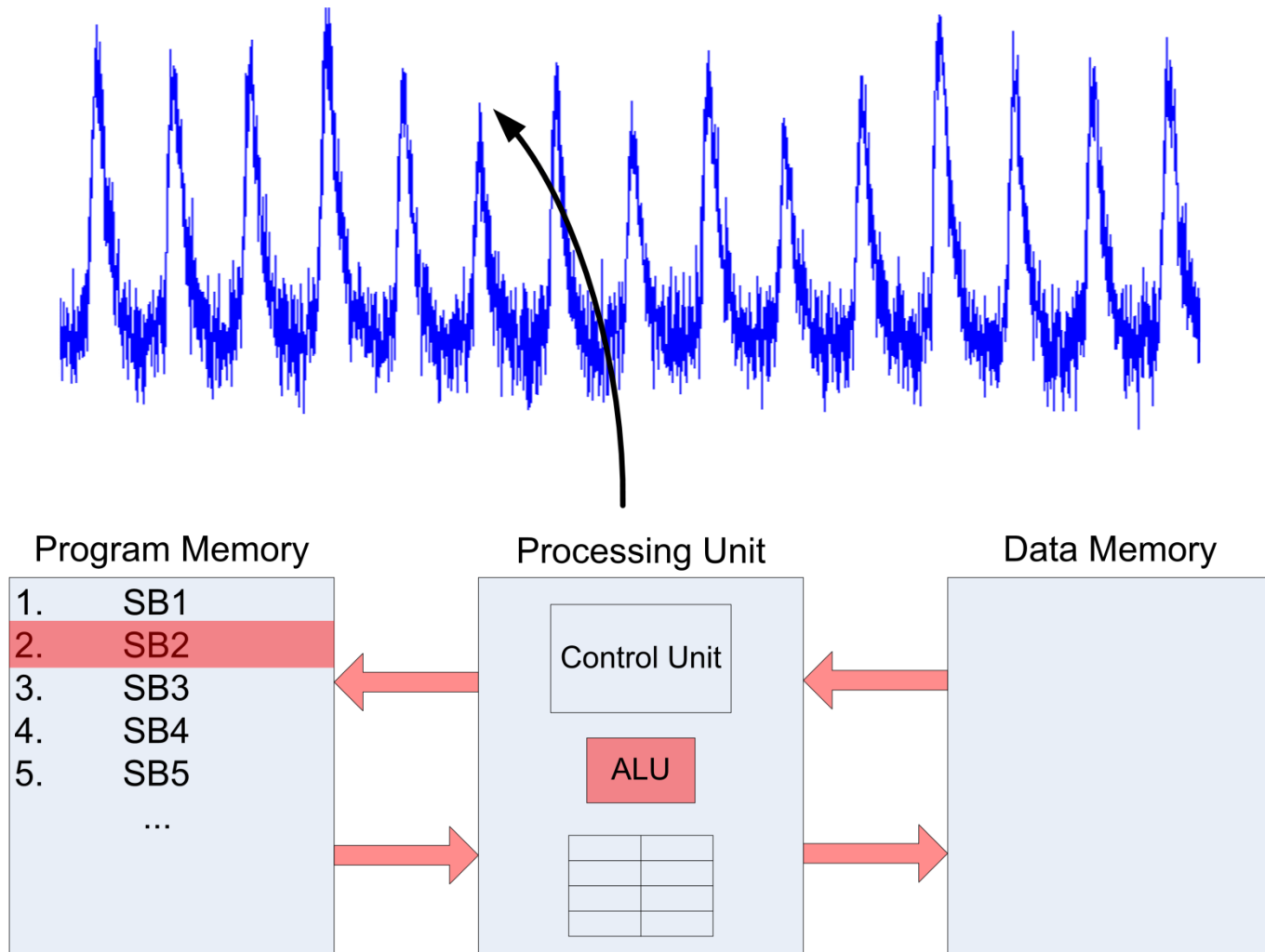
- Deterministic execution of the AES S-boxes



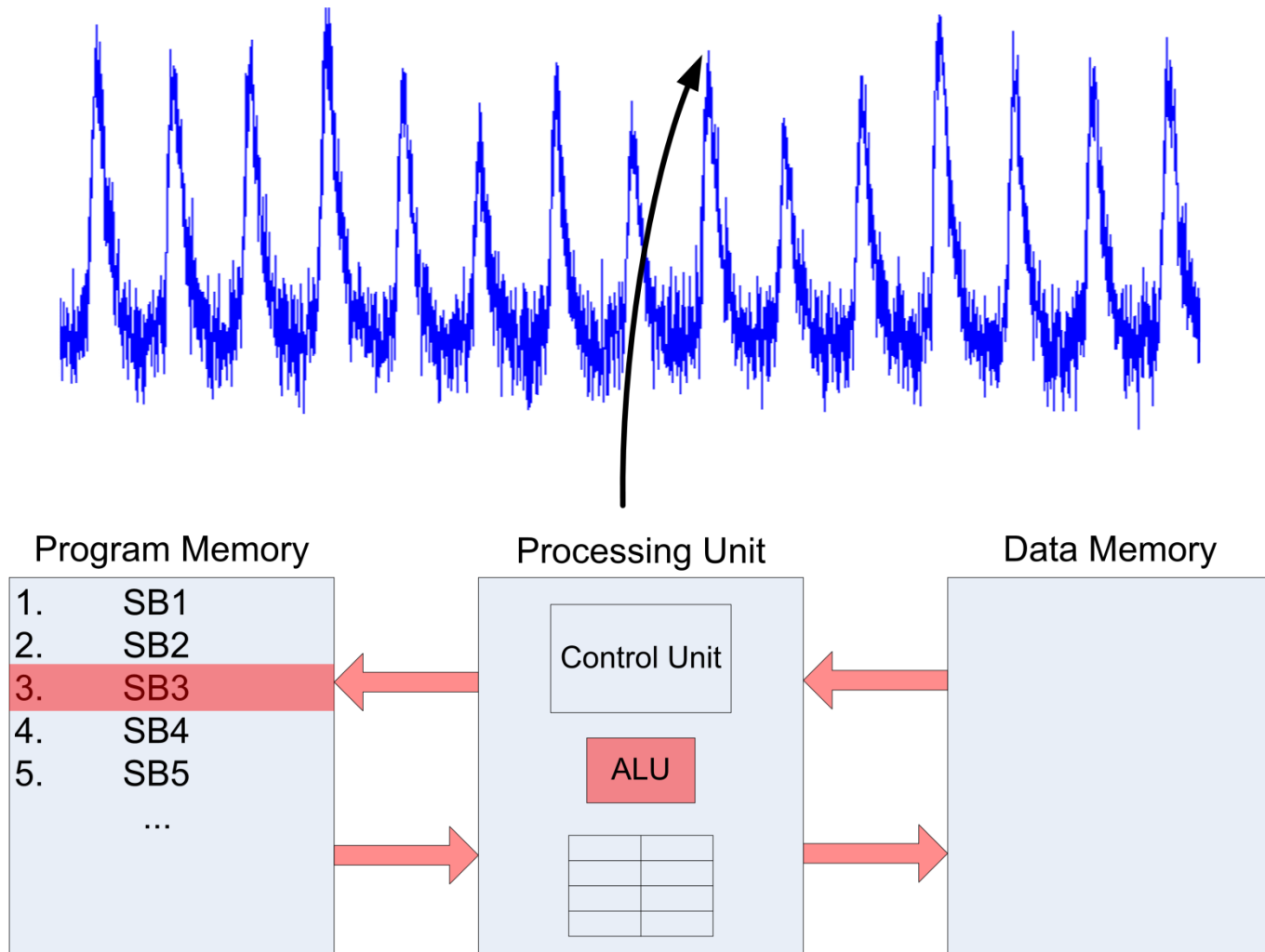
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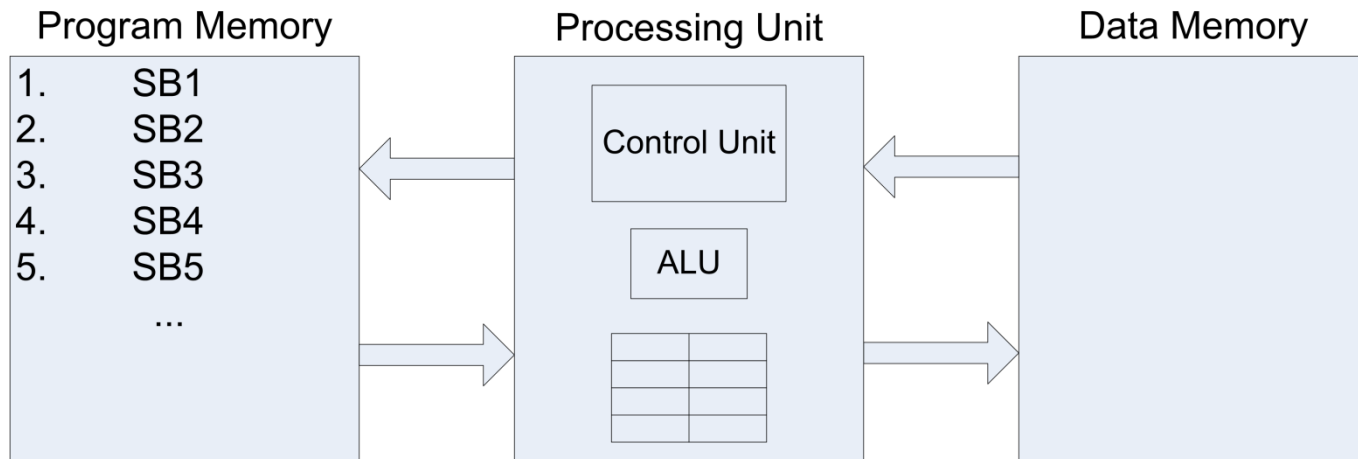
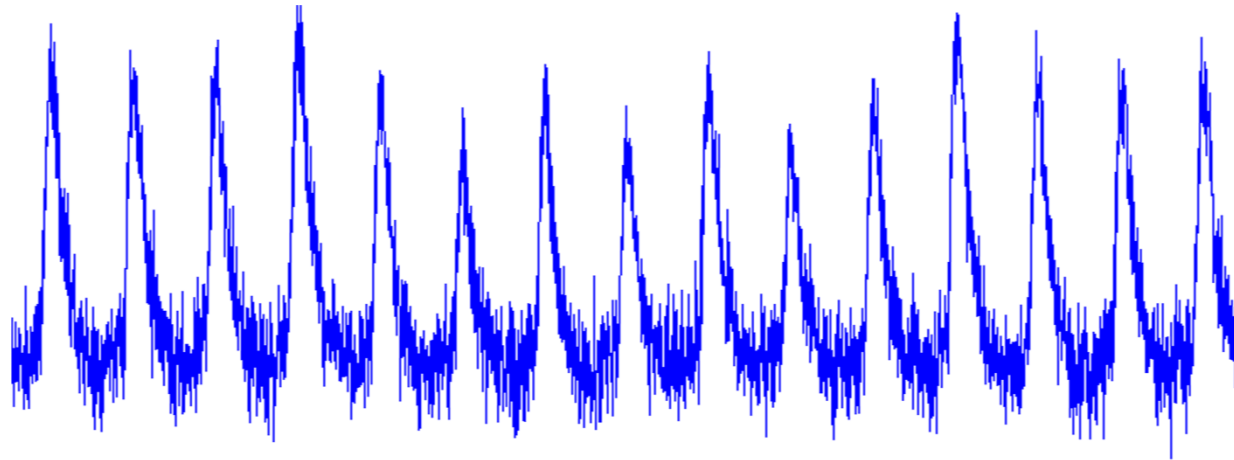
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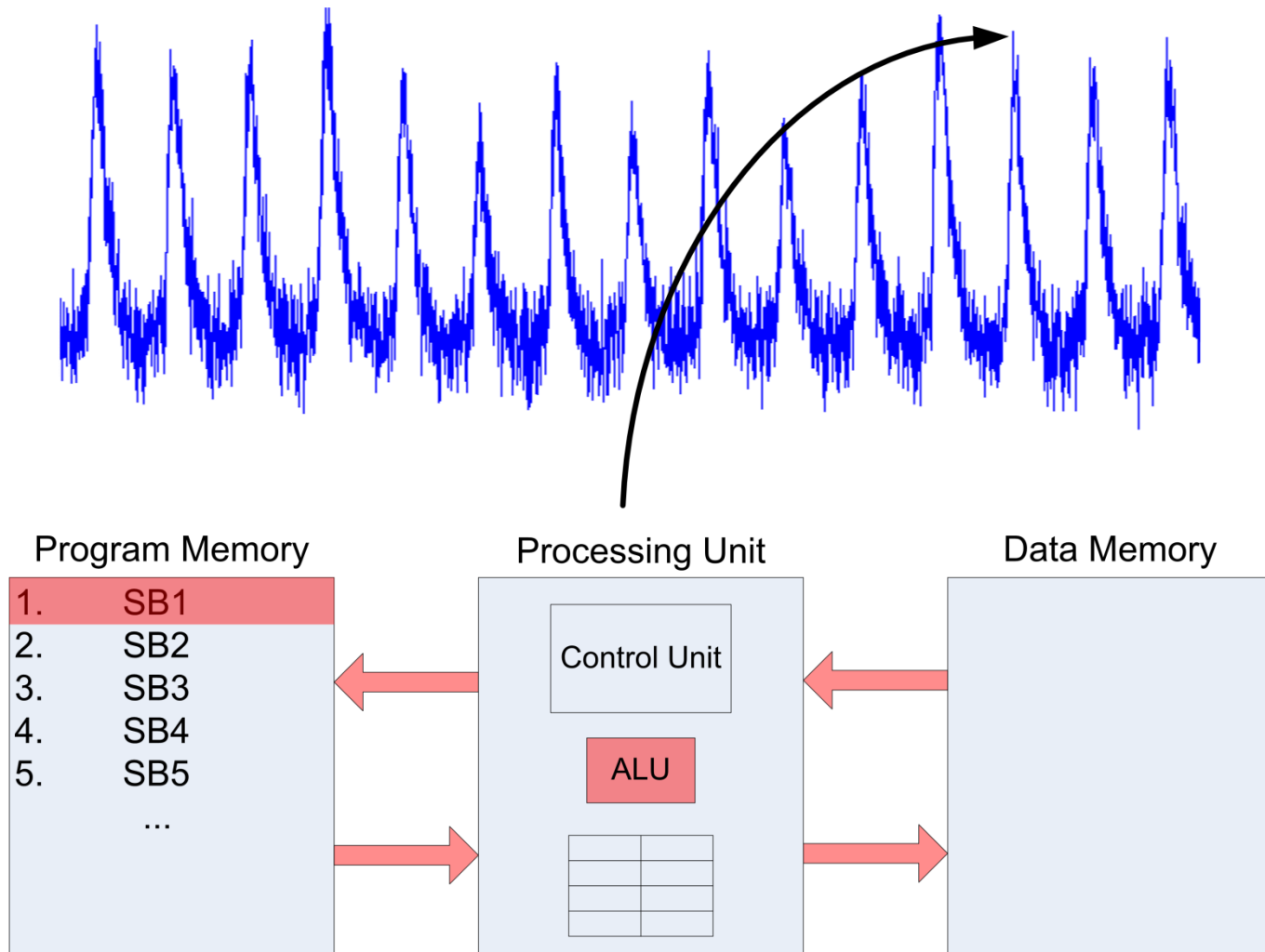
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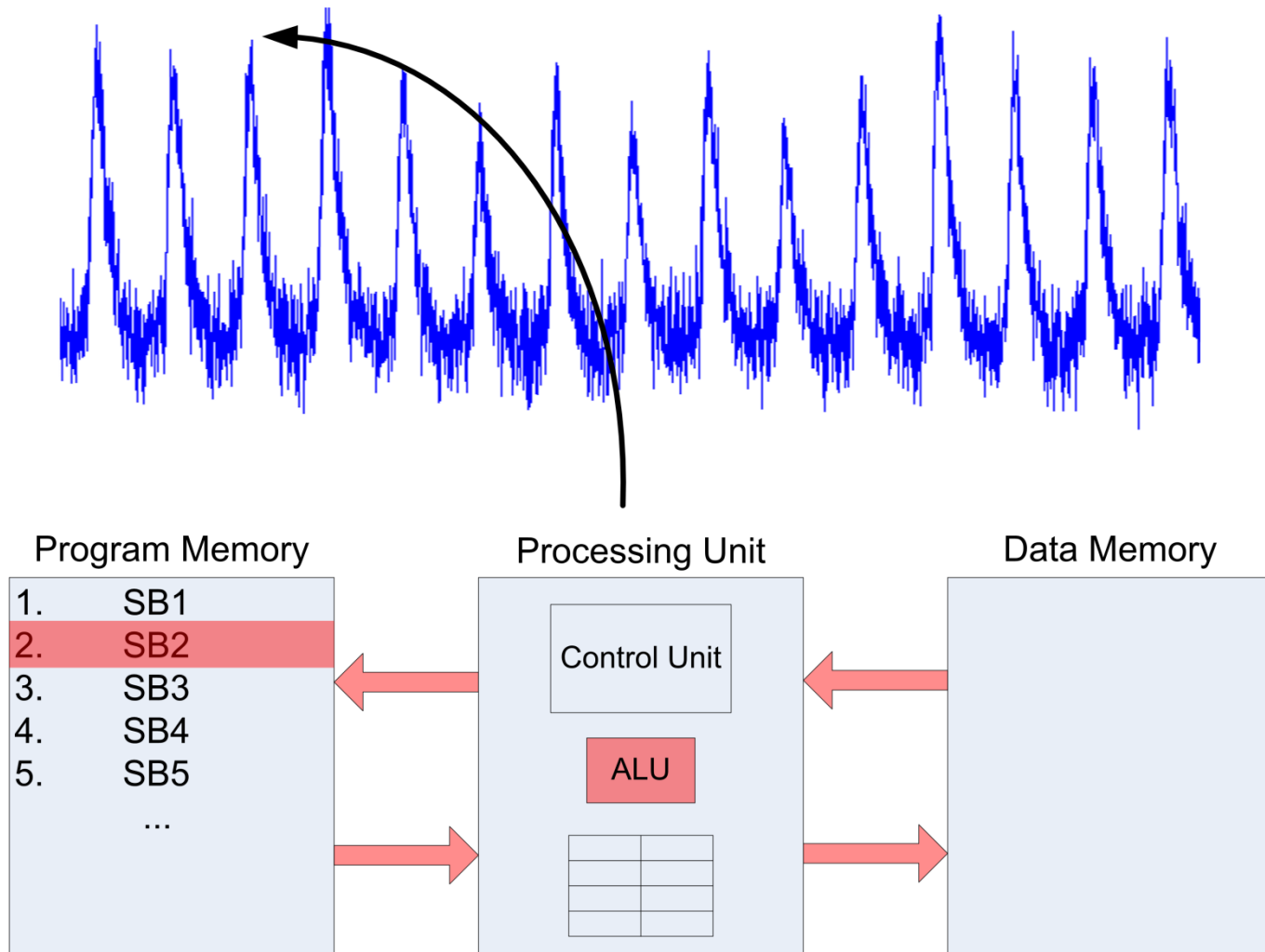
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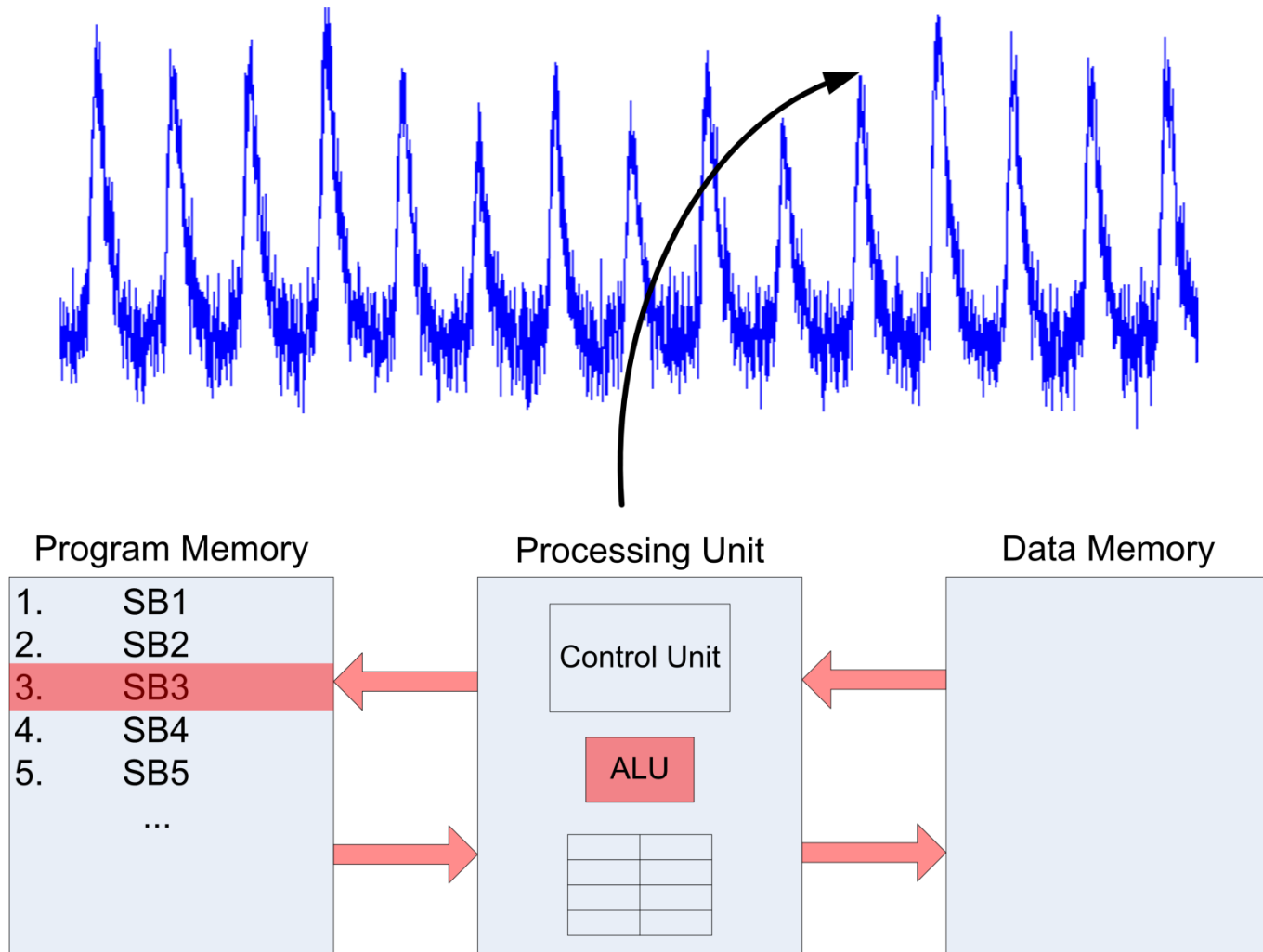
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⇒ Attack data complexity increases accordingly

Talk outline

1. Implementation: how to shuffle efficiently?
(Permutation generation - see paper)
 - a. Double indexing
 - b. (new) Randomized execution path
 - c. (new) Randomized program memory
2. Security evaluation: “better than integrating”
 - a. Information theoretic analysis
 - b. Actual chip measurements

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Shuffled AES :

Program Memory

1. Load shuffle index from memory
2. Load state byte from memory
3. SB(state(index))
4. Store state byte in memory
5. Load shuffle index from memory
6. Load state byte from memory
7. SB(state(index))
8. Store state byte in memory
- ...

Data Memory

Permutation

- | | |
|----|-----|
| 1. | 3 |
| 2. | 15 |
| 3. | 6 |
| | ... |

State

- | | |
|----|-------|
| 1. | byte0 |
| 2. | byte1 |
| 3. | byte2 |
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- Two RAM accesses per R/W access to operands
⇒ Very large cycle counts

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a. Information theoretic analysis

b. Actual chip measurements

Shuffled AES :
Program Memory

1. Generate shuffled address array
2. Find next instruction
3. Load state byte from memory
4. SB0
5. Find next instruction
6. Load state byte from memory
7. SB1
- ...

Data Memory

Permutation

1. 1
2. 15
3. 0
- ...

Address array

1. 6
2. 45
3. 3
- ...

State

1. byte0
2. byte1
3. byte2
4. byte3
- ...

Shuffled AES :
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Data Memory

Permutation

- | | |
|----|-----|
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| 3. | 0 |
| | ... |

Address array

- | | |
|----|-----|
| 1. | 6 |
| 2. | 45 |
| 3. | 3 |
| | ... |

State

- | | |
|----|-------|
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HOW?

Shuffled AES :
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7. SB1
- ...

Data Memory

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1.	1
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...	...

Address array

1.	6
2.	45
3.	3
...	...

State

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...	...

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Data Memory

Permutation

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3. 0
- ...

Address array

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2. 45
3. 3
- ...

State

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Permutation

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Address array

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Shuffled AES :

Program Memory

- | | |
|----|---------------------------------|
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Data Memory

Permutation

- | | |
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- | | |
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| 3. | 3 |
| | ... |

State

- | | |
|----|-------|
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| | ... |

- Better exploitation of registers
⇒ Significantly reduces the cycle count

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Shuffled AES :
Program Memory

1. Shuffle program memory
2. Load state byte from memory
3. SB0
4. Load state byte from memory
5. SB1
6. Load state byte from memory
7. SB2
8. Load state byte from memory
- ...

Data Memory

Permutation

1. 3
2. 15
3. 6
- ...

State

1. byte0
2. byte1
3. byte2
4. byte3
- ...

Shuffled AES :
Program Memory

1. Shuffle program memory
2. Load state byte from memory
3. SB0
4. Load state byte from memory
5. SB1
6. Load state byte from memory
7. SB2
8. Load state byte from memory
- ...

Data Memory

Permutation

- | | |
|----|-----|
| 1. | 3 |
| 2. | 15 |
| 3. | 6 |
| | ... |

State

- | | |
|----|-------|
| 1. | byte0 |
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| | ... |

Shuffled AES :
Program Memory

1.	Shuffle program memory
2.	Load state byte from memory
3.	SB3
4.	Load state byte from memory
5.	SB15
6.	Load state byte from memory
7.	SB6
8.	Load state byte from memory
	...

Data Memory

Permutation	
1.	3
2.	15
3.	6
	...

State	
1.	byte0
2.	byte1
3.	byte2
4.	byte3
	...

Shuffled AES :
Program Memory

1. Shuffle program memory
2. Load state byte from memory
3. SB3
4. Load state byte from memory
5. SB15
6. Load state byte from memory
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8. Load state byte from memory
- ...

Data Memory

Permutation

1. 3
2. 15
3. 6
- ...

State

1. byte0
2. byte1
3. byte2
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- ...

Shuffled AES :
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3. **SB3**
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Data Memory

Permutation

- | | |
|----|-----|
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State

- | | |
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Shuffled AES :

Program Memory

1.	Shuffle program memory
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3.	SB3
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Data Memory

Permutation

1.	3
2.	15
3.	6
	...

State

1.	byte0
2.	byte1
3.	byte2
4.	byte3
	...

- Large precomputations (technology dependent)
 - Somehow similar to a one-time program
- Minimum “online” cycle count (~ unprotected)

- Includes shuffling of other AES operations (among 16 for each of them – see paper for the details)

Implementation	Clock Cycles	
Unprotected AES	2739	(3546 with KS)
Double Indexing shuffling	30202	(46395 with KS)
Randomized Path shuffling	6934	(14834 with KS)
Randomized Memory shuffling	3299*	

* Excludes precomputations (approx. 18 milliseconds)

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⇒ Natural next step: include them in analysis

- Standard (sensitive operation) leakages

$$L_0 \leftarrow \text{Sbox}(k_{P(0)} \oplus X_{P(0)}),$$

$$L_2 \leftarrow \text{Sbox}(k_{P(2)} \oplus X_{P(2)}),$$

$$L_1 \leftarrow \text{Sbox}(k_{P(1)} \oplus X_{P(1)}),$$

...

- Standard (sensitive operation) leakages

$$\begin{aligned} L_0 &\leftarrow \text{Sbox}(k_{P(0)} \oplus X_{P(0)}), & L_1 &\leftarrow \text{Sbox}(k_{P(1)} \oplus X_{P(1)}), \\ L_2 &\leftarrow \text{Sbox}(k_{P(2)} \oplus X_{P(2)}), & &\dots \end{aligned}$$

- Let $S_c = P(c)$ be the part of the master key manipulated at cycle c , with P the shuffling perm.
- We additionally consider permutations leakages

$$L'_c \leftarrow S_c$$

- Based on the leakage probability distribution

$$\Pr[\mathbf{L} = \mathbf{l} | K_s = k] = \sum_c \frac{f(c, s, \mathbf{l}')}{\sum_{c'} f(c', s, \mathbf{l}')} \Pr[L_c = l_c | K_s = k]$$

- Based on the leakage probability distribution

$$\Pr[\mathbf{L} = \mathbf{l} | K_s = k] = \sum_c \frac{f(c, s, \mathbf{l}')}{\sum_{c'} f(c', s, \mathbf{l}')} \Pr[L_c = l_c | K_s = k]$$

- Different scenarios
 - Template attack without permutation leakage (UNI-TA)

$$f(c, s, \mathbf{l}') = 1/16$$

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- Different scenarios

- Template attack without permutation leakage (UNI-TA)

$$f(c, s, \mathbf{l}') = 1/16$$

- Template attack with permutation leakage (DPLEAK-TA)

$$f(c, s, \mathbf{l}') = \Pr[L'_c = l'_c | S_c = s]$$

- Based on the leakage probability distribution

$$\Pr[\mathbf{L} = \mathbf{l} | K_s = k] = \sum_c \frac{f(c, s, \mathbf{l}')}{\sum_{c'} f(c', s, \mathbf{l}')} \Pr[L_c = l_c | K_s = k]$$

- Different scenarios

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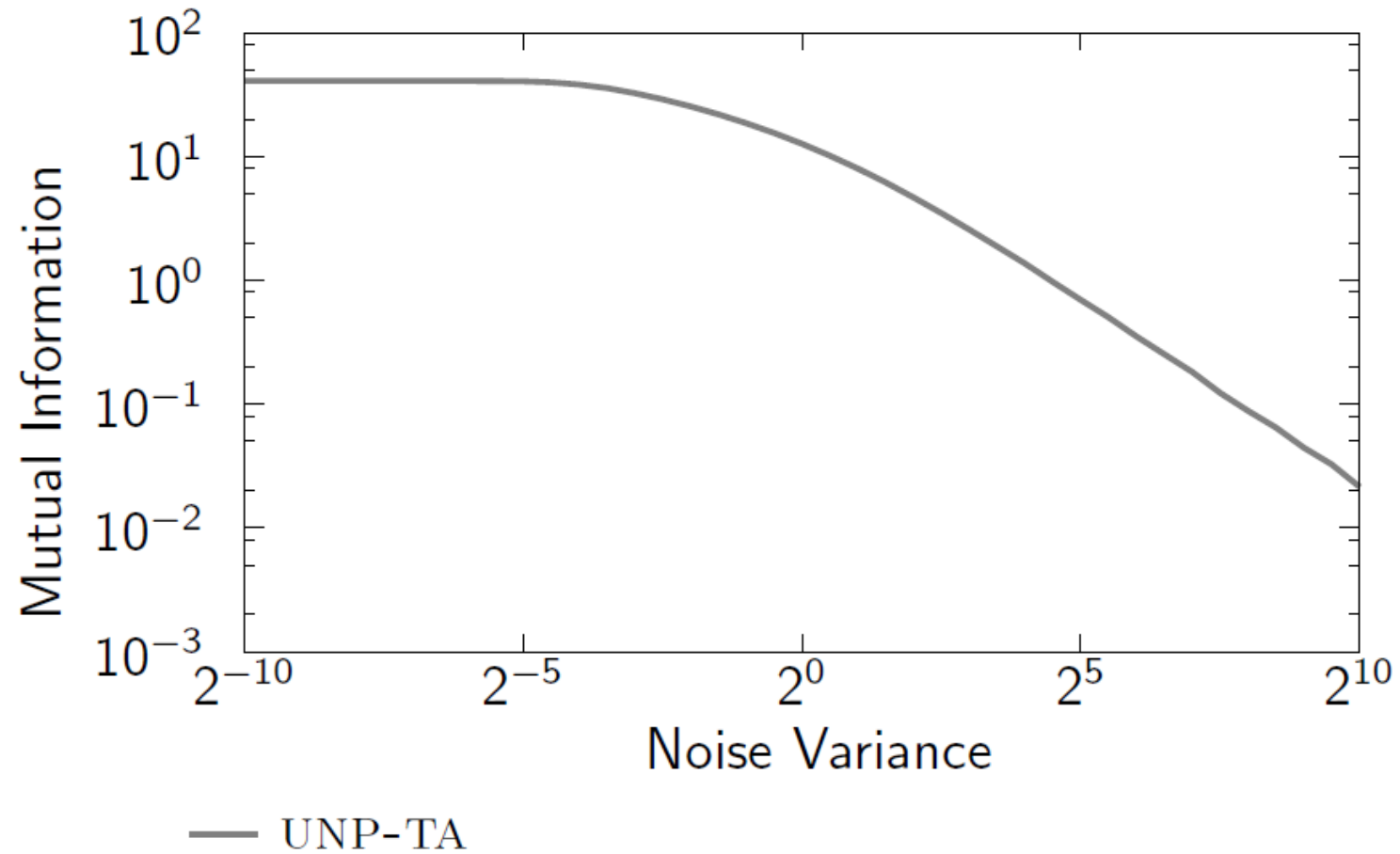
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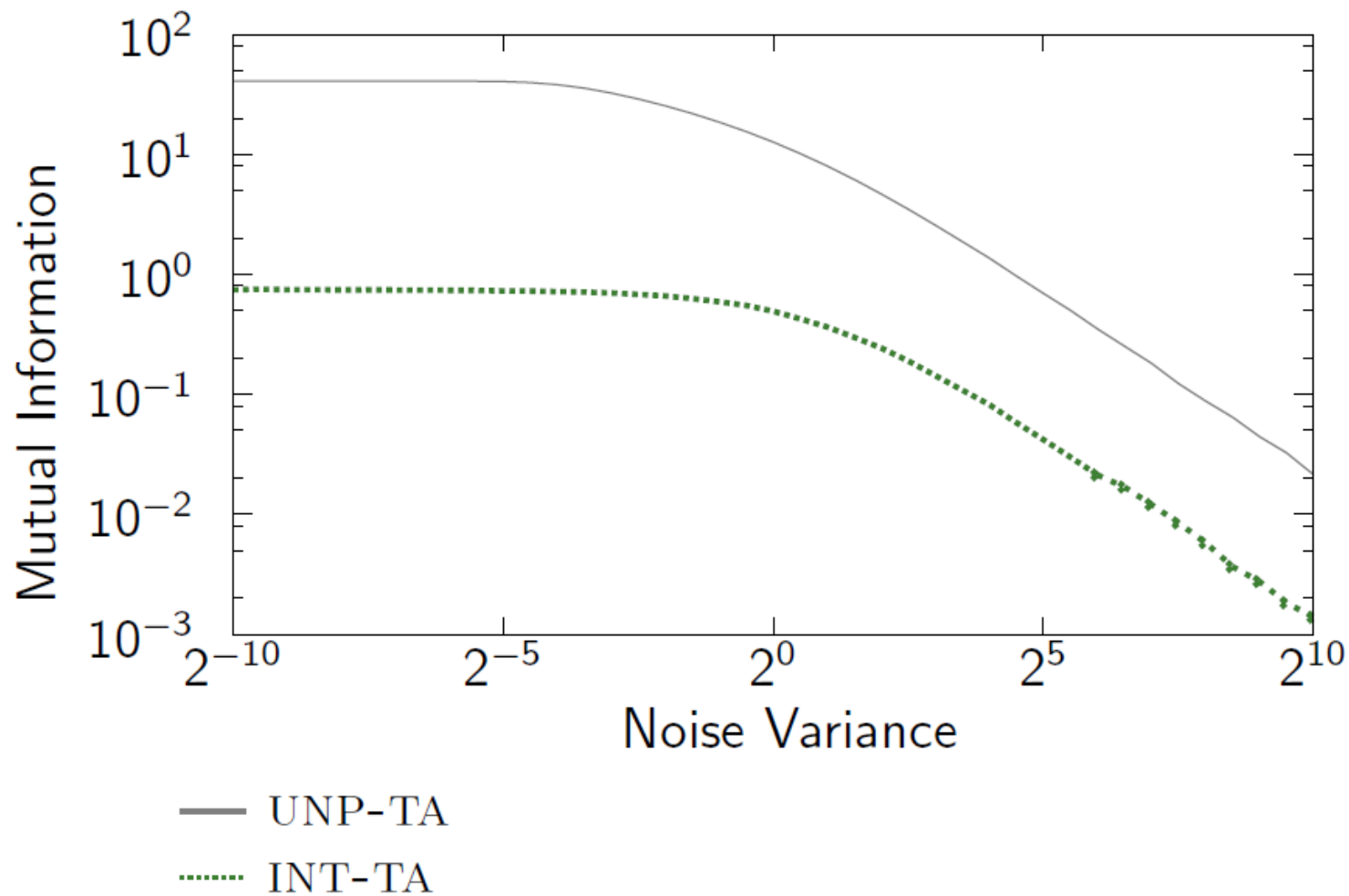
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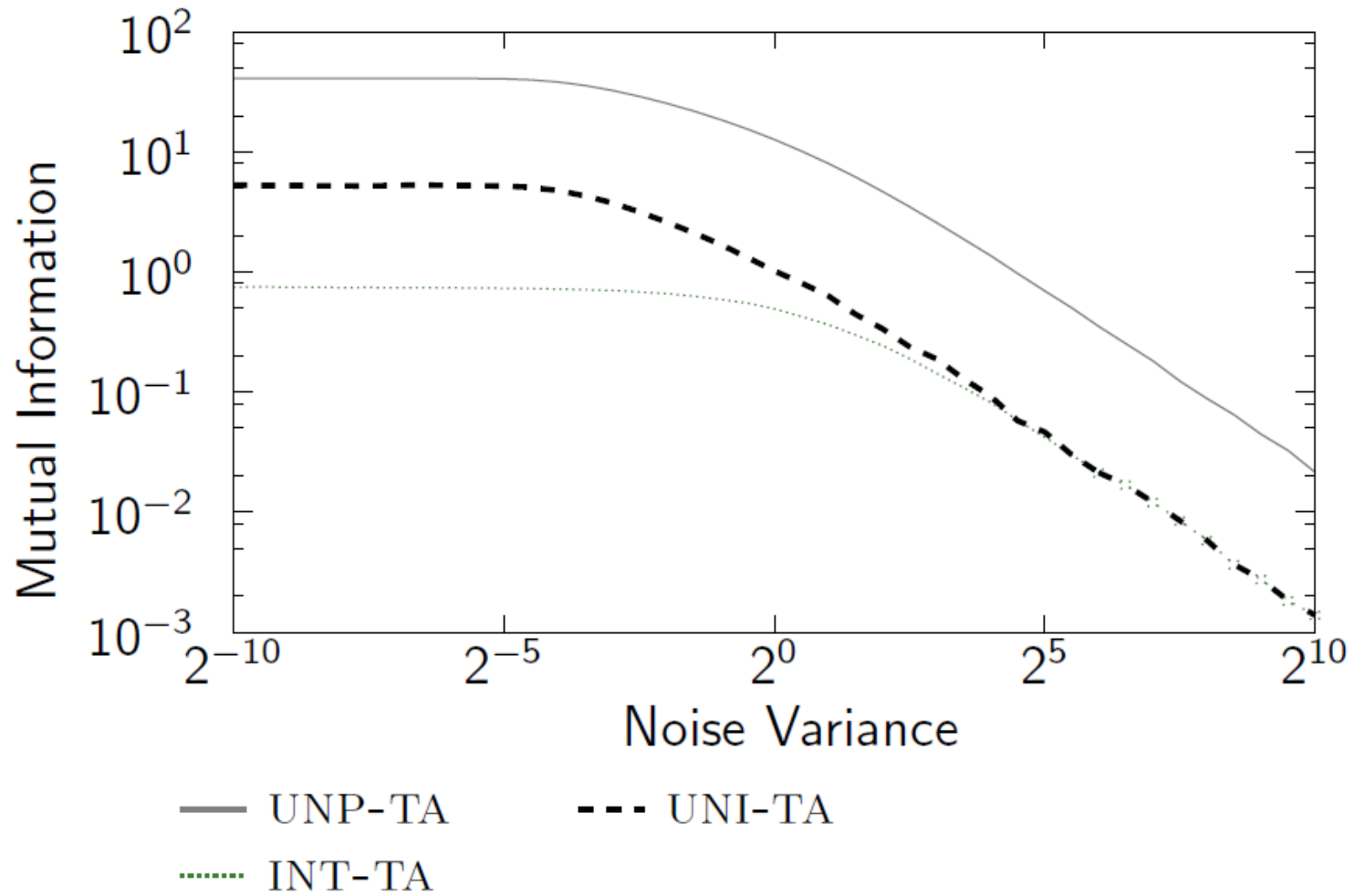
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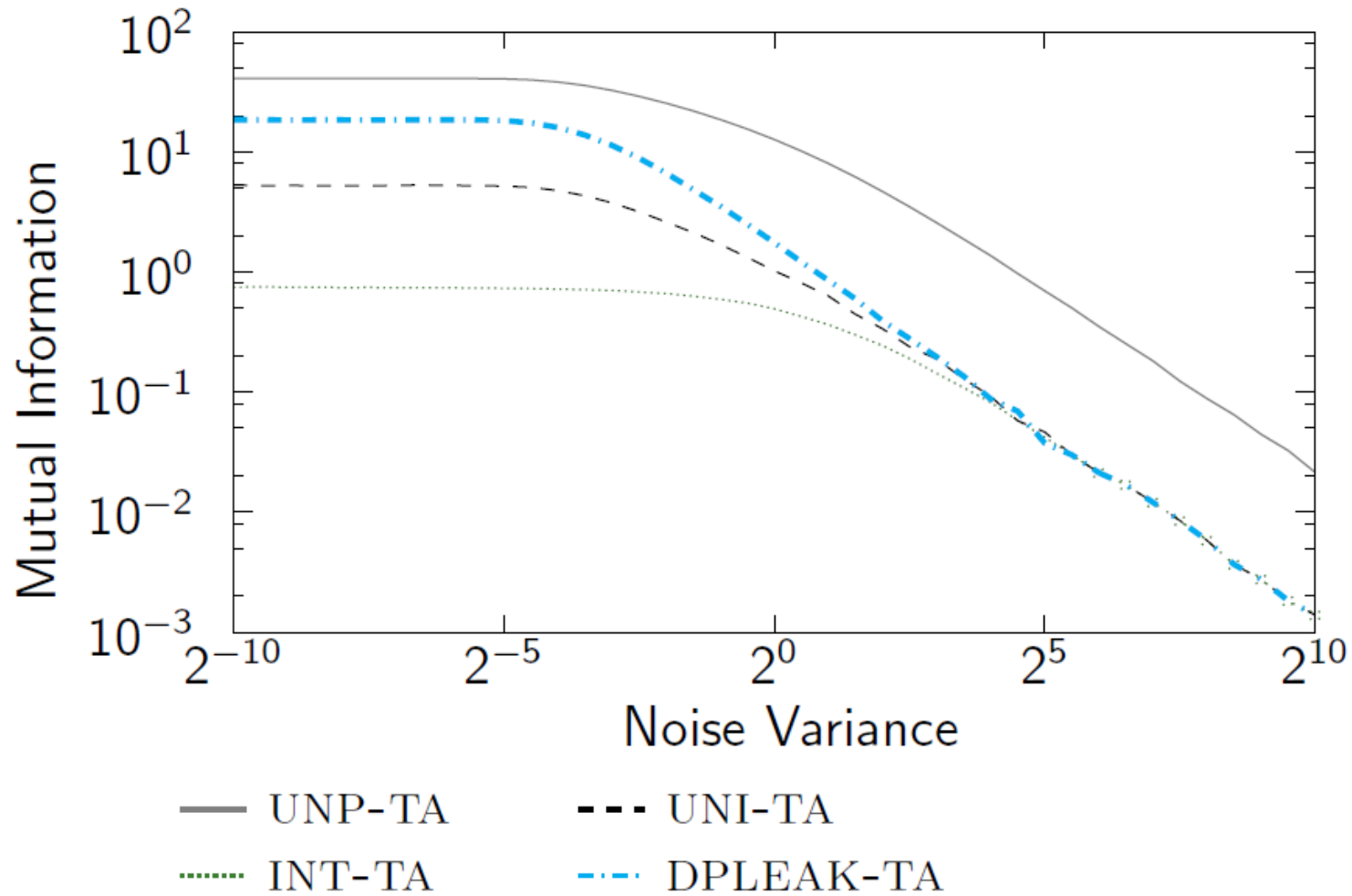
- Random Start Index (RSIENUM-TA)

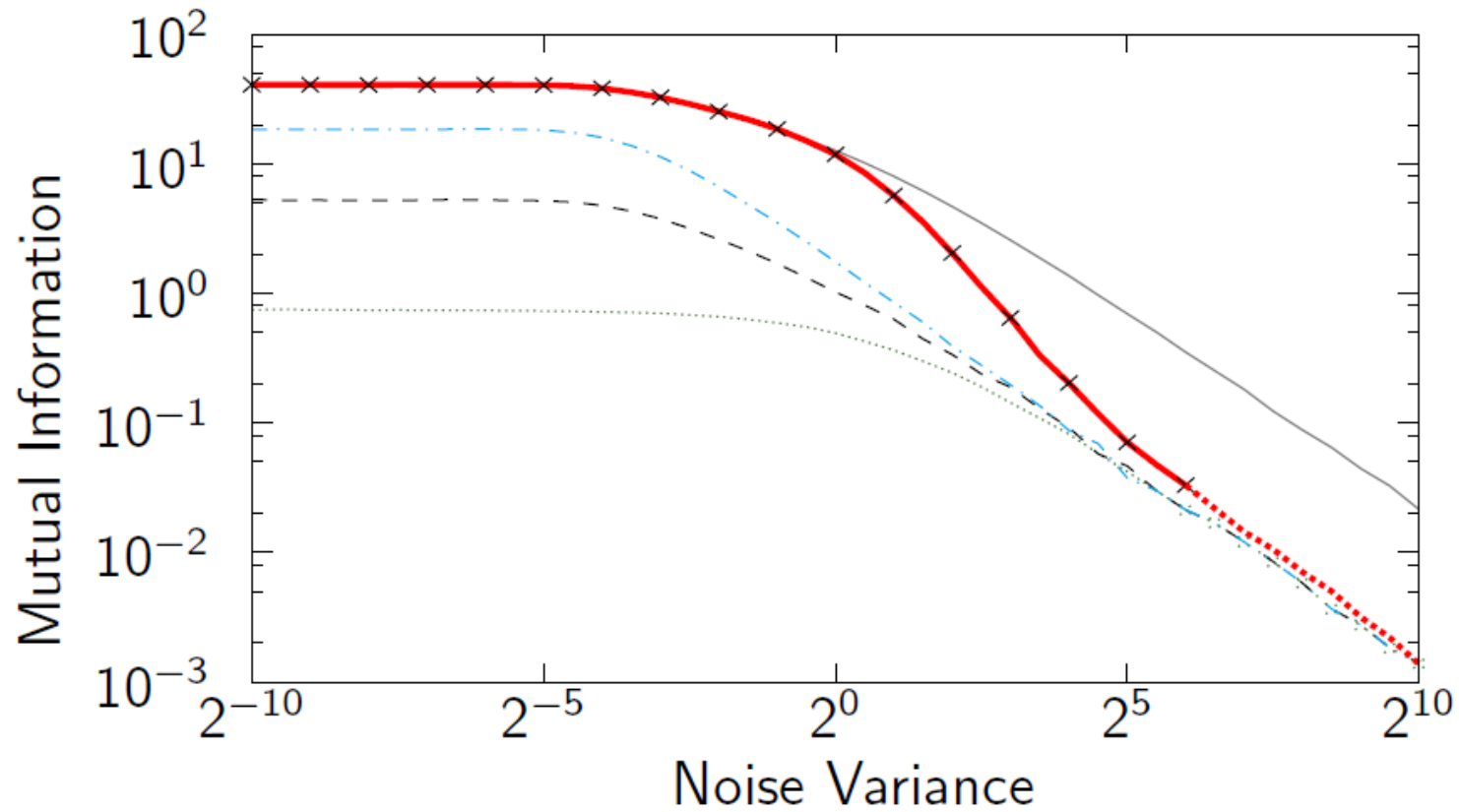
$$f(c, s, \mathbf{l}') = \prod_{i=0}^{15} \Pr[L'_i = l'_i | S_i = (s - c + i) \bmod 16]$$









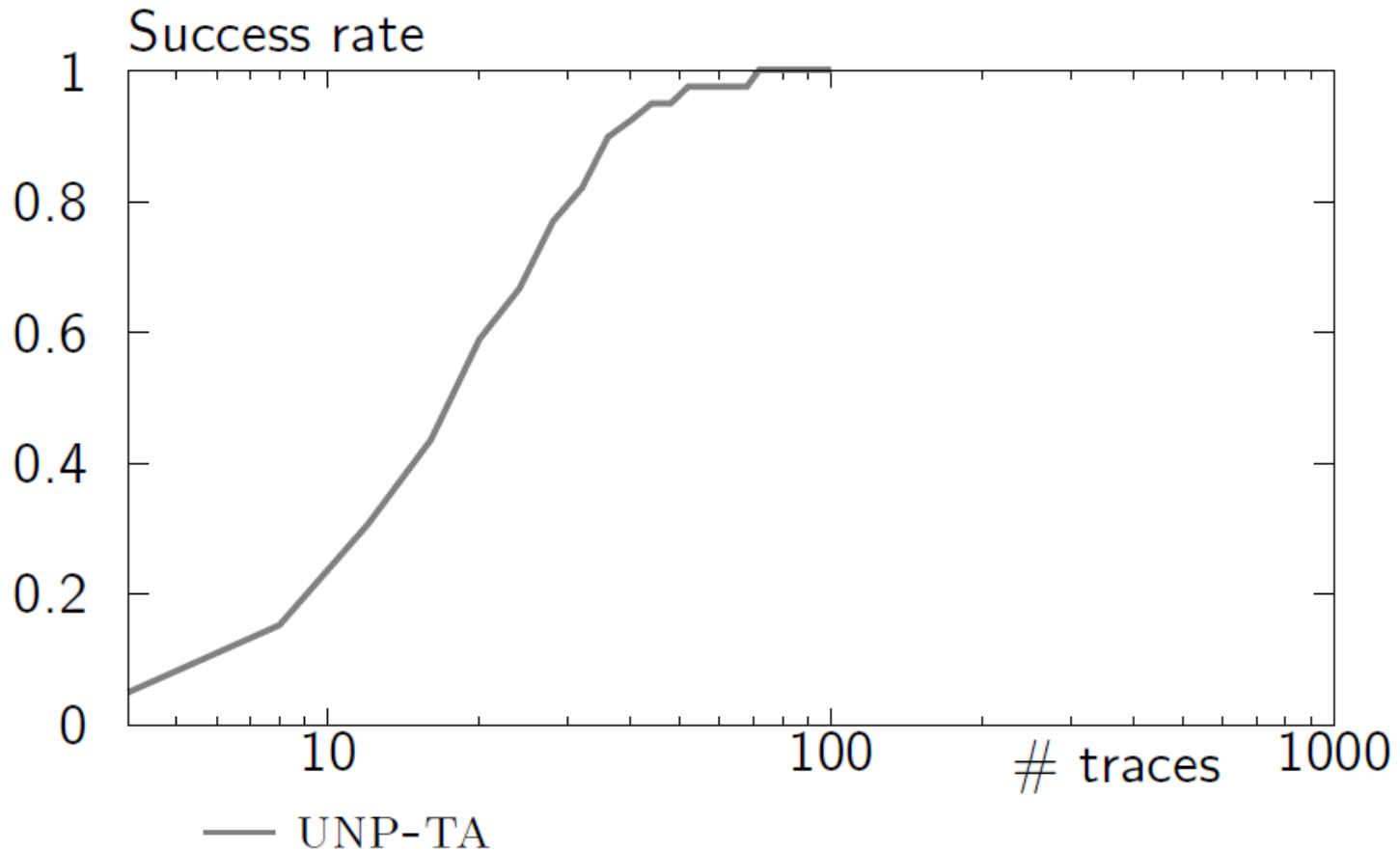


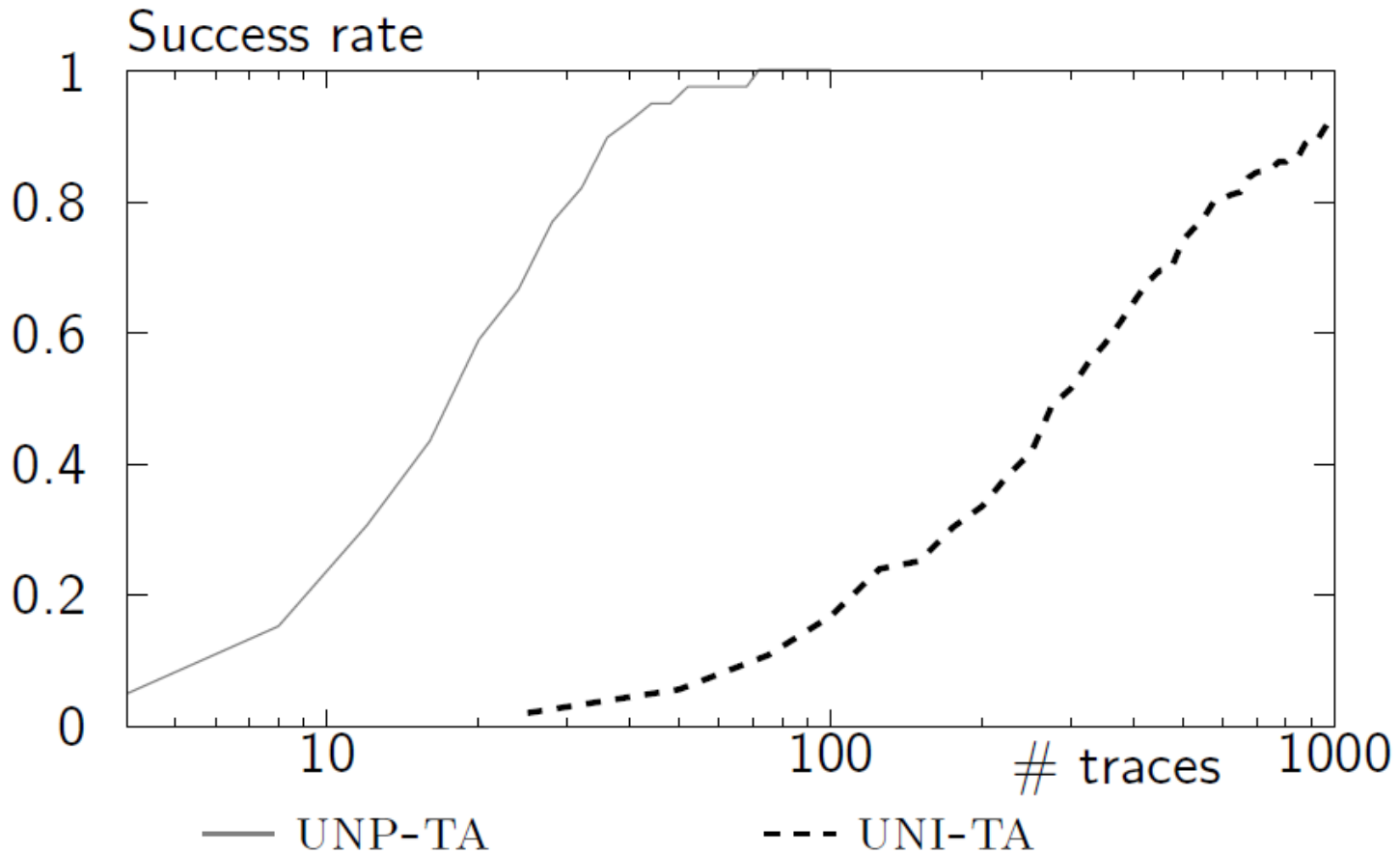
— UNP-TA - - - UNI-TA ×-× RSIENUM-TA
 INT-TA - · - · DPLEAK-TA

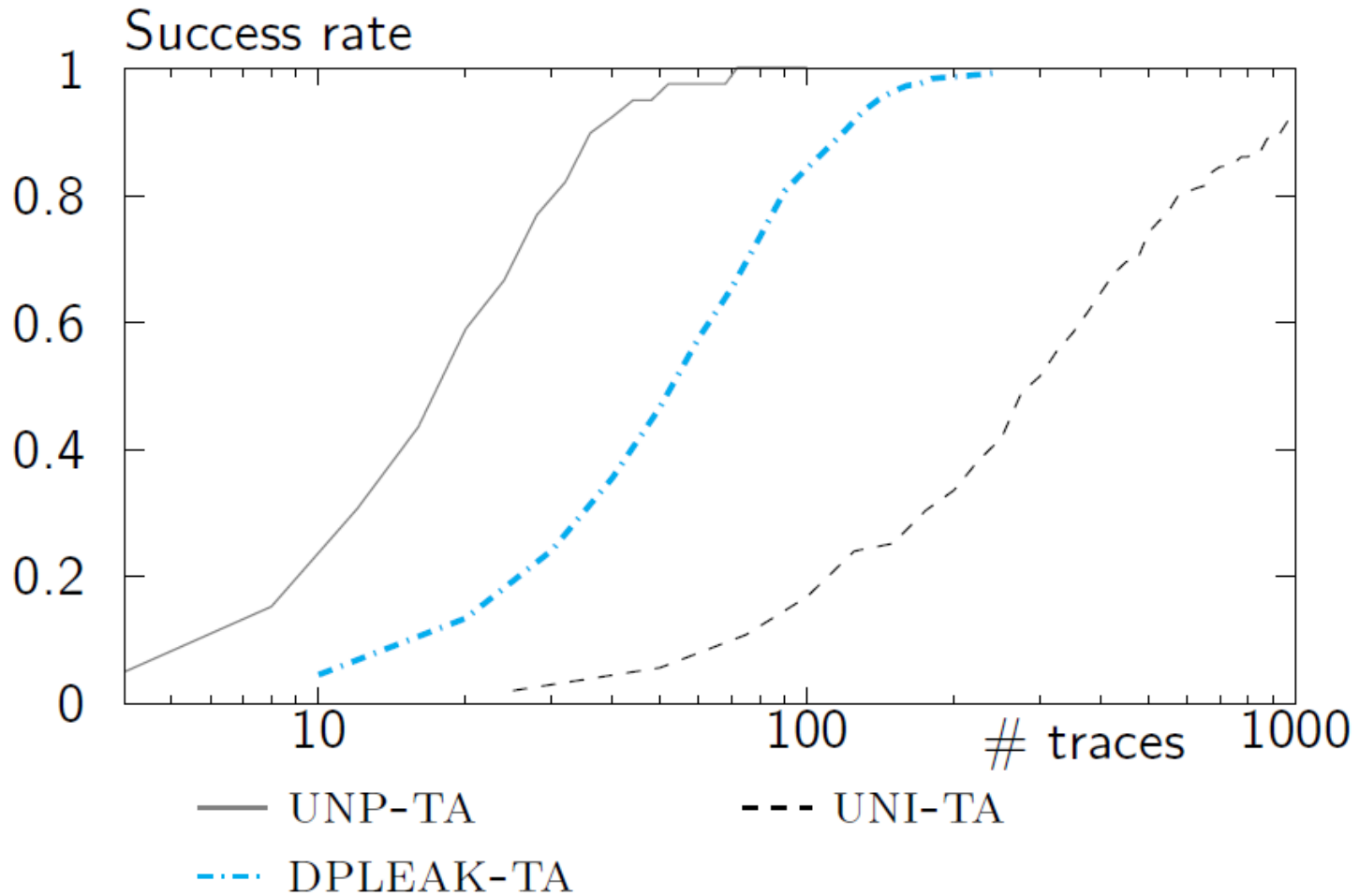
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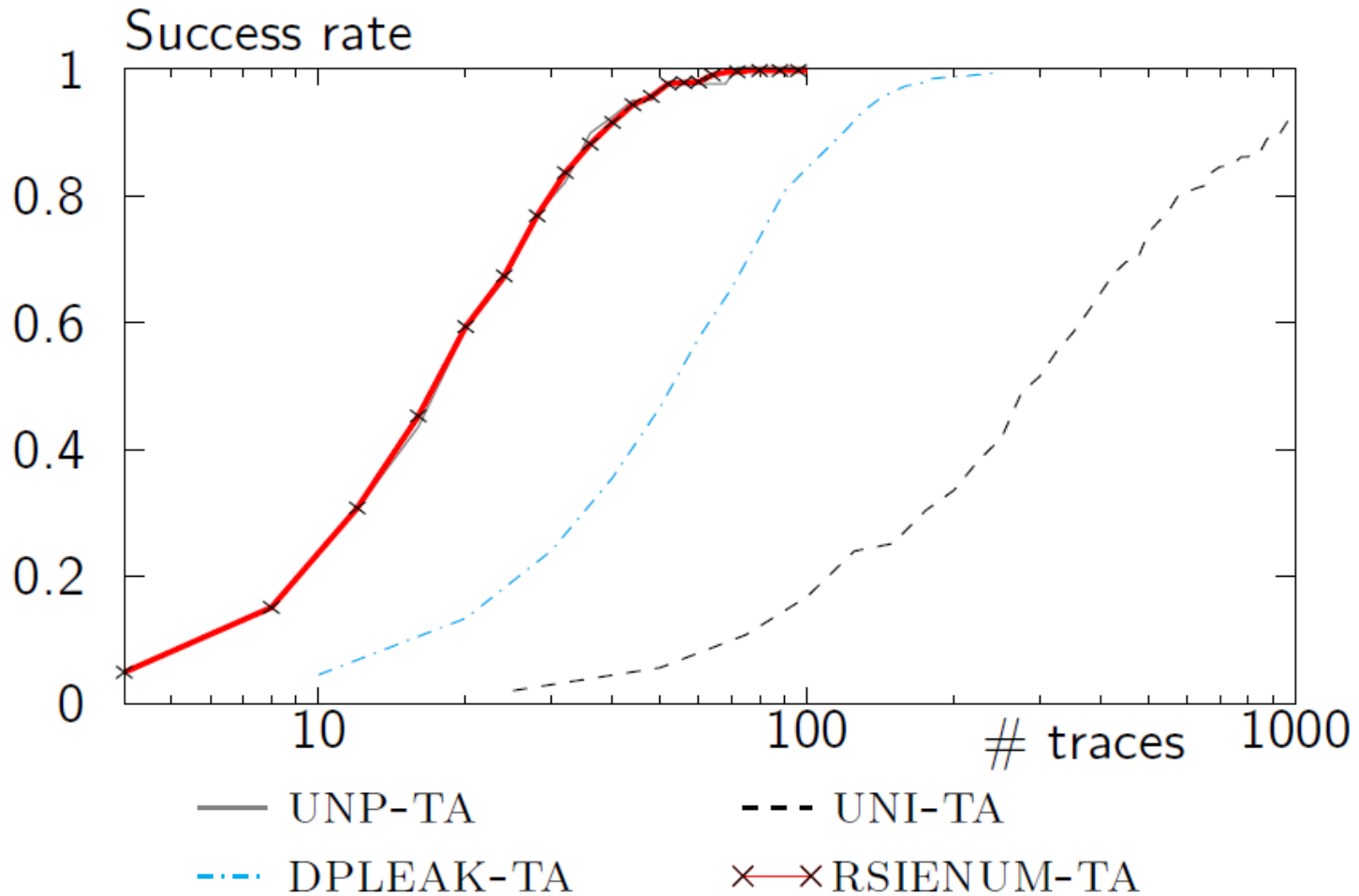
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- Why?

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 - Surprising since the opposite is usually observed (because simulated attacks have *perfect leakage models* while actual attacks use *estimated ones*)
- **Why? Recall the processor structure:**

Data Memory

Permutation

1.	3
2.	15
3.	6
	...

State

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2.	byte1
3.	byte2
4.	byte3
	...

- **Fact:** for similar amounts of noise, actual attacks more efficient than simulated ones
 - Surprising since the opposite is usually observed (because simulated attacks have *perfect leakage models* while actual attacks use *estimated ones*)
- **Why? Recall the processor structure:**
 - Even if operation order is shuffled, the state bytes are still manipulated by the same hardware resources!

Data Memory

Permutation

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 - *Even for randomized program memory !!*

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- Computation matters: enumerable permutations lead to easier attacks => RSI should be avoided
 - (and all the operations in the block cipher should be permuted over at least 16!)
- **Indirect leakages can appear!**
 - **Ideally, not only the order of operations should be shuffled, but also the resources used**

THANKS

<http://perso.uclouvain.be/fstandae/>